Doctoral Thesis

# A Study on Modulation Strategies of Dual Active Bridge DC–DC Converter for Battery Energy Storage Systems

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Doctoral Program in Advanced Electrical, Electronic and Computer Systems
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# A Study on Modulation Strategies of Dual Active Bridge DC–DC Converter for Battery Energy Storage Systems
# (蓄電池システムのための双方向絶縁型DC–DCコンバータの変調方式に関する研究)

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# Preface

The modulation strategy of the dual active bridge (DAB) dc–dc converter for the battery energy storage system (BESS) is investigated in this thesis. The challenges of operating in the BESS are identified. The suitable modulation strategies are reviewed and discussed. Since most of the modulation strategies have their limitations, the suitable modulation strategies are analyzed with an ideal DAB model. Based on the analysis, the first new modulation strategy is proposed and tested with the first prototype in a large voltage variation. The experimental results verified that the modulation strategy is suitable for the BESS. However, there is hard-switching operation at the low power range due to the parasitic elements. To operate in the soft-switching, the modulation strategy is analyzed with the parasitic elements. Based on the analysis, the second new modulation strategy is proposed and tested with the second prototype in large voltage variations. The experimental results show that the DAB dc–dc converter operates in soft-switching and has higher performance with the proposed modulation strategy at the low power range.

**Chapter 1** presents the global trend of electrical energy. Due to the intermittent nature of the renewable energies, a single renewable power generation has a low reliability. The energy storage systems (ESSs), especially the battery ESSs, increase the reliability of the renewable energies. The performance of BESS depends on the bidirectional dc–dc converter. Out of many bidirectional dc–dc converter, a dual active bridge (DAB) dc–dc converter is selected due to the natural soft-switching capability, bidirectional buck-boost operation, and simple circuit configuration. Based on the applications of the BESS, there are two challenges to operate the DAB dc–dc converter: large voltage variation and wide operational range.

**Chapter 2** investigates the suitable modulation strategies that operate in a large voltage variation and a wide operational range. From twelve modulation strategies, most of them have complex algorithm, neglected one degree of freedom, only one direction power transfer capability, and only buck capability. In order to overcome these issues, DPWM and SPWM are analyzed with a lossless DAB dc–dc model. Based on the analysis, both modulation strategies are combined and a new modulation strategy, combined pulse-width modulation (CPWM), is proposed to enable the bidirectional power flow and the boost operations. The CPWM algorithm includes all the three degrees of freedom and the interval classification for the positive and negative power. CPWM is tested with the first prototype in a large voltage variation condition. The experimental results verify that CPWM operate in a wide power range and suitable for the BESS. In addition, the efficiency of CPWM is higher than that of phase shift modulation (PSM). However, hard-switching operation is found in the low power range of CPWM (DPWM) due to the parasitic elements.

**Chapter 3** investigates the effect of parasitic components and dead time in the DAB dc–dc converter model and in DPWM. The parasitic components cause the additional snubber losses during the hard-switching operation. To operate in the zero voltage switching (ZVS), DPWM is analyzed with the parasitic elements. Based on the analysis, the tunable dual pulse-width modulation (TDPWM) strategy is proposed to perform the ZVS for buck and boost conditions. TDPWM is tested with the second prototype in the low power transfer and in large voltage variation conditions. The experimental results verify that the DAB converter operates in the ZVS. In addition, the efficiency of TDPWM and DPWM are compared. The experimental results show that TDPWM has higher efficiency than DPWM in buck/boost conditions.

**Chapter 4** concludes the presented work and provides an outlook regarding future research.

# 1. Introduction

## 1.1. Global trend of electrical energy

The environment, power sustainability, and geopolitical concerns have resulted in a revolution in the energy sector towards a renewable energy future including wind turbines and photovoltaic (PV) systems. However, the intermittent nature of these renewable energies introduces issues with system stability, reliability, and power quality. These issues can be addressed by implementing energy storage systems (ESSs) in power system or alongside with these renewable energy systems. In the ESSs market and research, the battery energy storage systems (BESSs) are gaining momentum due to their power flexibility ranging from kilowatts to megawatts [1], [2].

The BESS is a system that stores electrical energy in batteries in the form of chemical energy. The stored chemical energy can also be released as electrical energy to support the utility grid or renewable energies. The performance of a BESS is strongly affected by the power electronics technologies.

### 1.1.1. Global energy consumption trend

Global energy consumption trend is the total energy used by the entire world in the 21st century. The global energy consumption is expected to grow by 41% from 575.4 quadrillion Btu in 2015 to 813.7 quadrillion Btu in 2050 (Fig. 1.1) [3]. The rise of the consumption is caused by the enhanced living standards of developed countries and expanding world population. In 2018, the world population has reached 7.6 billion people [4]. However, the percentage of people who have accessed to modern energy is 87% [5]. The households without access to the modern energy, including clean cooking facilities and electricity, are often considered as poverty. In this situation, the women spend more times in cooking and washing clothes than in educating children and supporting the society. Hence, the country with a lack of access to sustainable and reliable modern energy faces difficult challenges in handling poverty, air pollution, lack of quality education, and economic growth [5]. Everyone should have the access to the modern energy.

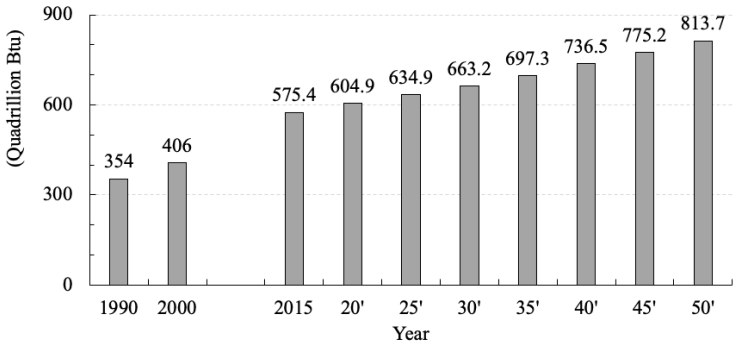



Fig. 1.1. Global energy consumption, 1990–2050 [3].

On the other hand, most of the modern energy are generated from conventional sources such as fossil fuels. The increase consumption of the modern energy will result in increased of greenhouse gasses. The greenhouse gasses, such as carbon dioxide, in the atmosphere is responsible for the global warming effect which changes the climate and weather [6]. Climate change leads to the increase frequency of natural disasters, the emergence of new diseases, and the re-emergence of extinct diseases [7]. In addition, the fossil fuel takes millions of years to produce which is not sustainable for long term usage.

### 1.1.2. Renewable energy trend

Renewable energy trend is the total renewable energy used by the entire world in the 21st century. Fig. 1.2 shows the global renewable generation capacity in 2017 was estimated 178 gigawatts more than the previous year, which is the largest annual increase. The global warming effect and sustainable energy issues have resulted a revolution in the energy sector towards a renewable energy future. Overall, the net growth of the renewable energies was estimated 70% of global energy capacity in 2017 [8]. The net growth of solar photovoltaic and wind power generation capacity alone is greater than that of coal, natural gas, and nuclear power combined.

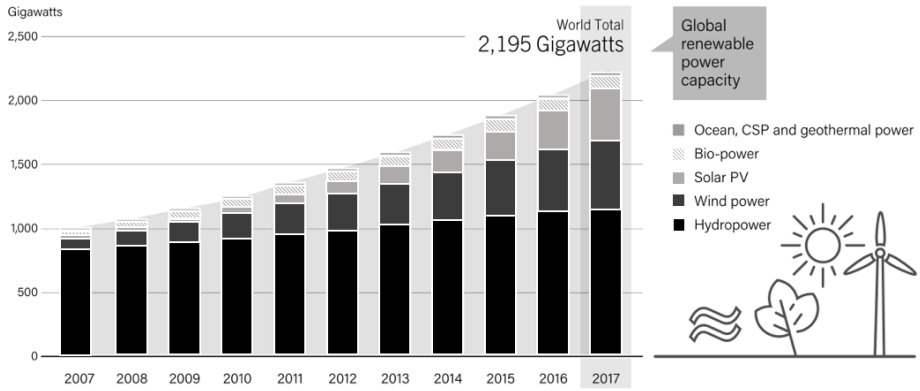



Fig. 1.2. Global renewable power capacity, 2007-2017 [8].

The reasons behind this increase are the cost reduction of the enabling technologies, the significant investment in developing and developed countries, and the renewable energy policies. The total global investment in renewable power in 2017 was at least USD 310 billion which was 2% higher than 2016. The value of investment in new renewable power capacity was three times the investment in fossil fuel. Majority of the investment is in photovoltaic and wind power [8].

Table 1.1 summarized the top 5 ranking of the annual investment in the renewable energy [8]. China has the most share in the global investment followed by US. Some of developing and emerging countries overtook developed countries especially in biodiesel and ethanol productions.

Table 1.1. Top 5 ranking of annual investment in 2017 [8].

| | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| Investment in renewable power and fuels (excluding hydro over 50 MW) | China | United States (U. S.) | Japan | India | Germany |
| Geothermal power capacity | Indonesia | Turkey | Chile | Iceland | Honduras |
| Hydropower capacity | China | Brazil | India | Angola | Turkey |
| Solar PV capacity | China | U. S. | India | Japan | Turkey |
| Wind power capacity | China | U. S. | Germany | United Kingdom | India |
| Biodiesel production | U. S. | Brazil | Germany | Argentina | Indonesia |
| Ethanol production | U. S. | Brazil | China | Canada | Thailand |

### 1.1.3. Energy storage system (ESS) trends

The energy storage system (ESS) is the enabling technology that increases the reliability of renewable energy [1]. U.S. and China have also invested considerably in utilizing energy storage systems (ESS) for their system networks. By 2015, the U.S. had installed 21 GW of energy storage systems by 2015 [9]. Meanwhile, China had successfully installed a total of 22.85 GW of energy storage systems by 2015 [9]. These developments show how much ESS are advancing in parallel with the renewable energy.

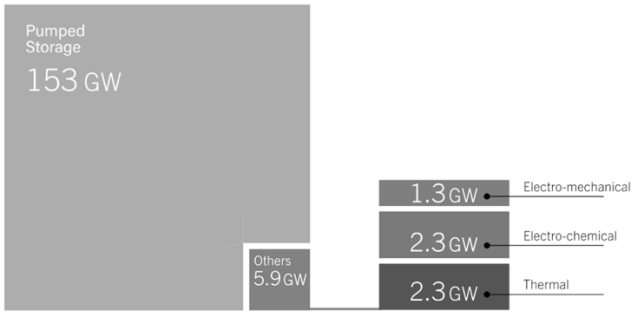



Fig. 1.3. Global energy storage capacity in 2017 [8].

Fig. 1.3 shows the global utility-scale ESS capacity totaled an estimated 159 GW, with pumped hydro energy storage (PHES) accounting for the vast majority (153 GW) [8]. PHES is followed by thermal storage, then by battery (electro-chemical) and electro-mechanical storage. PHES is widely used because it is an early technology that is industrially practical for power system. PHES has the largest power capacity of ESS and is suitable to balance power in the distribution grid. However, PHES requires a significant capital investment and occupies large space.

Thermal storage systems (TSSs) capture heat, generated with electricity or from thermal energy sources, for later use. TSS is useful in extremely hot and cold climate countries [10]. Although the TSS is efficient and reliable, the market for TSS remains small [8].

Electro-chemical energy storage or BESS are mostly installed in distribution grids. In China, the capacity of BESSs installed in distribution grids is the largest (40%), followed by that in renewable energy integration (20%) [9]. In United States, majority of the BESSs are also installed in distribution grids to provide an ancillary services [9].

Residential and commercial (behind-the-meter) electricity storage capacity, in places with supporting regulatory structures, also grew rapidly in 2017 such as Germany, Australia, Japan, China, and US [11]–[13]. In Germany and Australia, they install solar PV systems with ESS to maximize solar power self-consumption [14].

The BESS have wide applications in utility grids and residential areas, ranging from kilowatts to megawatts. Due to the power flexibility, the BESSs are gaining momentum in researches and industries [1], [2]. Especially, Li-ion batteries are gaining momentum in the electric power industry [15]. They are also widely used in electric vehicles (e.g., Tesla Model S, Chevrolet Bolt EV, Nissan Leaf) and consumer electronic products (e.g., laptops, smart phones). Fig. 1.4 shows that a price survey of Li-ion batteries, where the electric production cost has dropped –72% in 2016 than that in 2010 [16]. The cost reduction makes the Li-ion BESS an interesting solution to increase the reliability of the renewable energy systems.

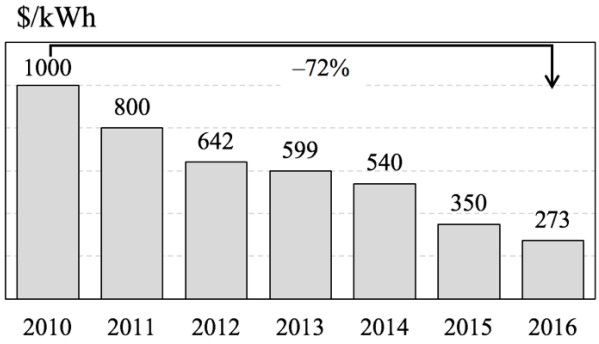



Fig. 1.4. BNEF Li-ion battery price survey [16].

## 1.2. Applications of BESS with renewable energies

There many types of a renewable energy such as solar, wind, hydro, marine, geothermal, and bioenergy [17]. Two popular renewable energies are discussed in this section, which are wind turbines and photovoltaic (PV) systems.

### 1.2.1. Wind energy system

Wind energy system is a system that converts kinetic energy from wind through wind turbines into electric energy. The wind turbine technology have been transformed dramatically [18]. Especially, the size varies from small to large scale. The size is chosen based on the average wind speed and the output power. The wind turbine technology had reached to a point that it can be integrated fully with power converters (Fig. 1.5) [19]–[21]. All the generated power from the wind turbine can be regulated. Even in a large-scale wind energy system (>3 MW), the power converters such as the multicell converter are able to transfer all the power into the grid [22].

However, a single wind turbine system is not reliable to generate energy. Fig. 1.6 shows a typical power output profile of a large wind farm. The power output has steep rises and sudden drops. Fig. 1.7 shows wind energy system with BESS. Fig. 1.8 shows typical power output profile of a large wind farm with BESS. The power output is smoother in this configuration. The power in the BESS has wide power variation between –1.5 kW to 1.5 kW.

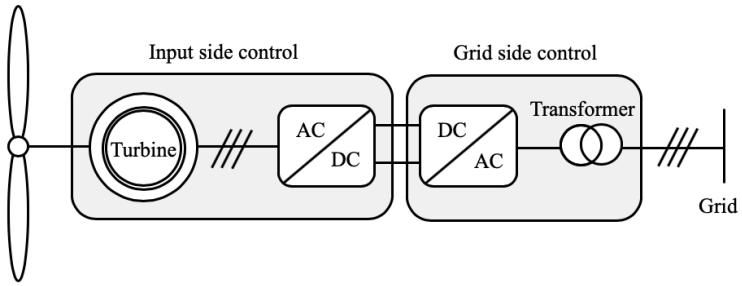



Fig. 1.5. Wind turbine systems with full scale power converter [19]–[21]

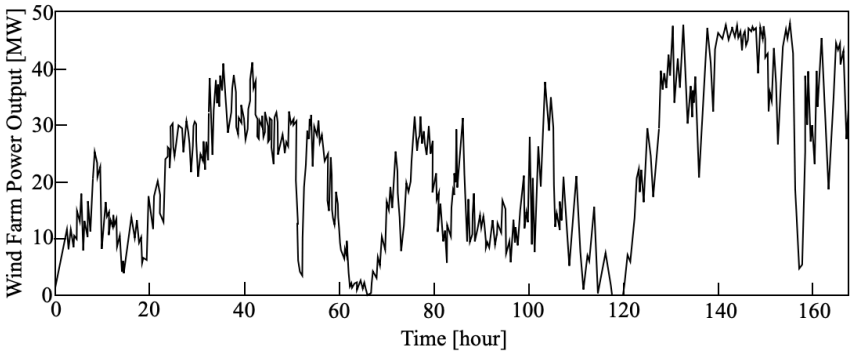



Fig. 1.6. Typical large wind farm power output [23].

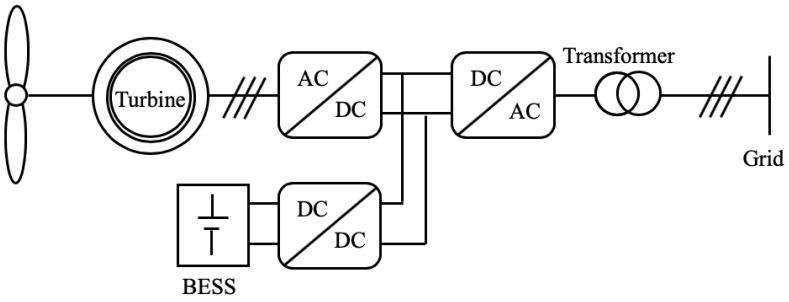



Fig. 1.7. Integrated wind energy system with BESS [20].

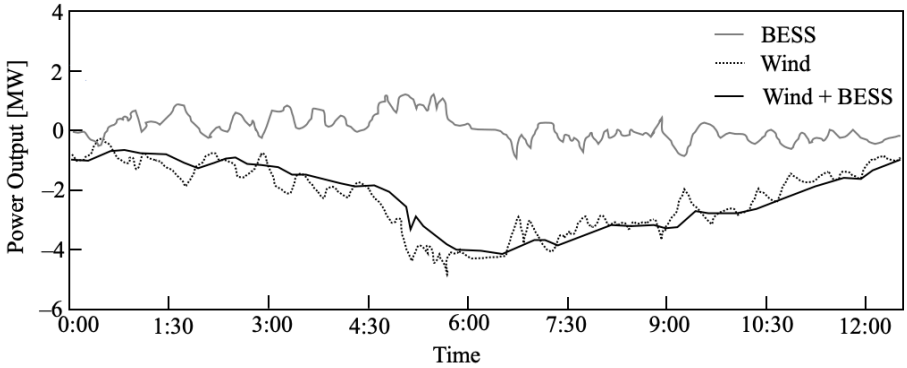
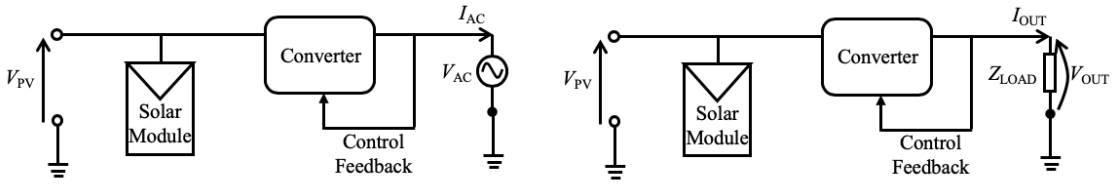



Fig. 1.8. Smoother output power (black line) from wind power energy output (dotted line) and battery energy storage system (grey line). [24].

### 1.2.2. Photovoltaic (PV) system

A photovoltaic system is a system that generates electricity when exposed to sunlight. Unlike wind turbine system, which needs to undergo several stages, photovoltaic system can directly generate electricity anywhere as long as the sunlight is available. There are several topologies to harness the energy from PV system [25]. Fig. 1.9 shows that PV modules can either be connected to the grid or they can be used as isolated power supplies.

The output patterns of PV systems also depend on the weather [26]. Fig. 1.10 shows the PV power output patterns for three different weather types (sunny, rainy, and cloudy days). This irregular power output can disturb the stability of the whole power system.




(a) (b)

Fig. 1.9. PV energy applications. (a) Grid-connection. (b) Isolated power-supply [25].

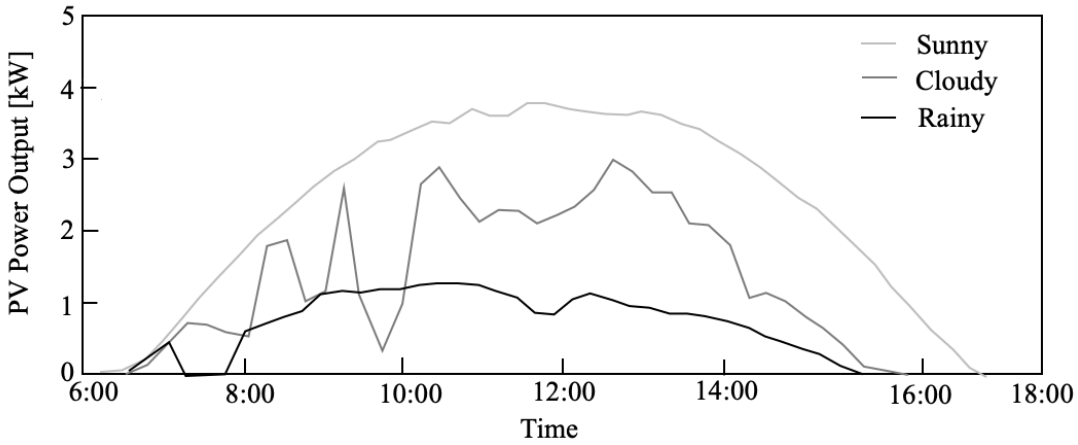



Fig. 1.10. PV power generation patterns for three different weather types [26].

### 1.2.3. Hybrid energy systems

Neither the wind energy systems nor the PV systems can provide a continuous and reliable supply of energy due to seasonal and periodical climate variations. To solve these issues, hybrid energy systems are implemented where the PV and wind energy systems are combined with BESS. Fig. 1.11 shows the hybrid energy system where these systems are connected at the dc bus. In a typical battery energy storage system (BESS) a bidirectional dc-dc converter is essential to transfer power between the battery and the dc bus.

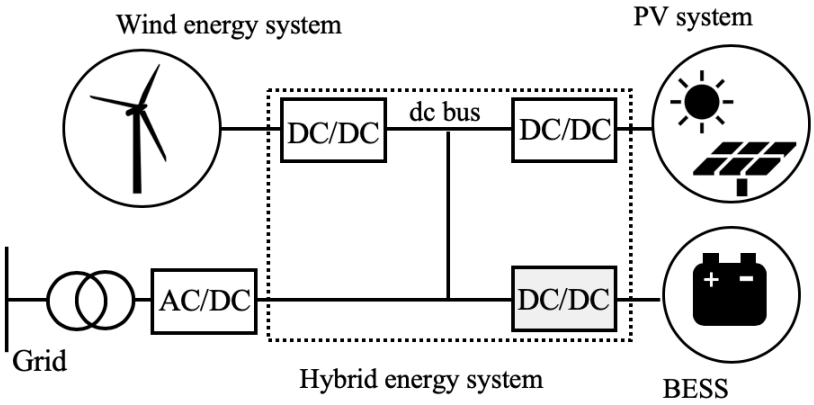



Fig. 1.11. Hybrid energy system connected to a grid.

### 1.2.4. Bidirectional DC–DC converter

Bidirectional dc–dc converter is an electronic circuit that bidirectionally transfer power in the form of direct current (dc). There are two types of bidirectional dc–dc converters: isolated and non-isolated. The efficiency of non-isolated converters is usually higher than isolated converters. If large voltage gain is required, the non-isolated converters require more switches, bigger inductors, and bigger capacitors [27]–[29]. Since the BESS has large voltage gain, the isolated dc–dc converters are preferred. The isolated dc–dc converters can easily achieve large voltage gains by adjusting the winding ratio of the transformer. Furthermore, an isolated converter is safer and more reliable. A typical isolated bidirectional converter is shown in Fig. 1.12. There are many types of isolated converters including flyback type [30]–[31], forwad-flyback type [32]–[34], half bridge type [33], and full bridge type [34]. In this study, a single-phase dual active bridge (DAB) dc-dc converter is chosen because of its soft-switching capability, bidirectional buck-boost operation, and simple circuit configuration [34].

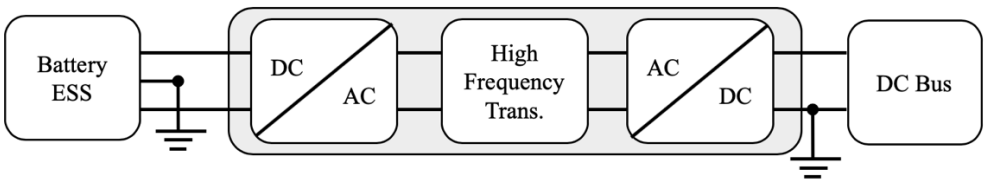



Fig. 1.12. Isolated bidirectional dc–dc converter.

## 1.3. The objective and new contributions of this study

In the hybrid energy system, there are two main challenges to operate the DAB dc–dc converter in the BESS. The **first challenge** is a battery has a large voltage variation. Every rechargeable battery has a different nominal, maximum, and minimum voltage. Fig. 1.13 shows the voltage variation of a cell of lithium-ion battery according to state of charge (SOC) during charging and discharging [35]. The voltage

variation is larger in a battery pack that has many cells connected in series. In this study, the primary side of the BESS is considered as the dc bus and the secondary side of the BESS as the lithium batteries. The paper only considered the condition where the voltage of the dc bus is more than the lithium batteries.

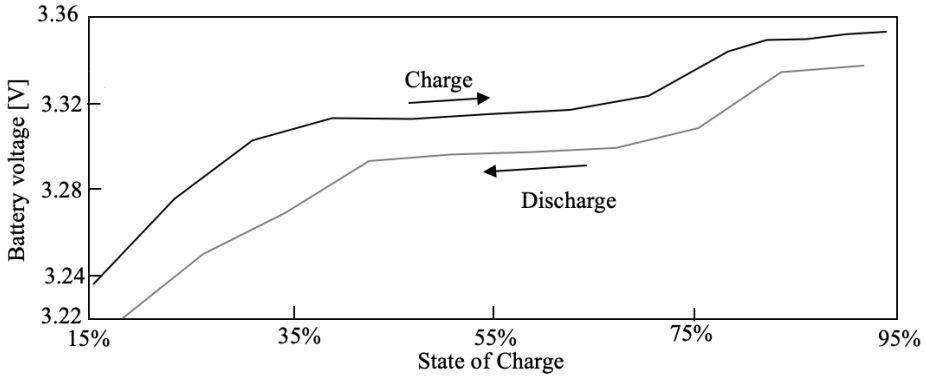



Fig. 1.13. Voltage variation in a cell of lithium-ion battery during charging and discharging [35].

The **second challenge** is photovoltaic (PV) systems and wind power systems have a wide operational range. From the power output of the PV system in Fig. 1.10, two operating conditions of the BESS are identified and summarized in Table 1.2.

Table 1.2. Operating conditions of the BESS

| Conditions | Weather | Power range |
|---|---|---|
| high | Sunny | –2 kW to 2 kW |
| low | Rainy | –0.4 kW to 0.4 kW |

The **research objective** of this study is to improve the efficiency of the DAB dc–dc converter when the BESSs have a large voltage variation and a wide operational range. These lead to several new contributions such as:

- Proposal of a simple modulation strategy with bidirectional, buck, and boost capability[1].
- Proposal of a parasitic PWM waveforms used to analyze the modulation strategy and to estimate the zero-voltage switching (ZVS) conditions.

[1] Based on this modulation strategy, a journal paper has been published as M. H. Azmeer bin Ab Malek, Kakigano H., and Takaba K, "Combined Pulse-Width Modulation of Dual Active Bridge DC-DC Converter to Increase the Efficiency of Bidirectional Power Transfer", IEEJ Transactions on Industry Applications, vol. 7, no. 2, pp. 167–174, March 2018.

- Proposal of a simple modulation strategy with the ZVS capability in the low power range[2].

[2] Based on this modulation strategy, a journal paper has been published as M. H. Azmeer bin Ab Malek, Kakigano H., and Takaba K, "Dual Active Bridge DC–DC Converter with Tunable Dual Pulse-Width Modulation for Complete Zero Voltage Switching Operation", IEEJ Transactions on Industry Applications, vol. 8, no. 1, January 2019.

# 2. Simple Modulation Strategy with Bidirectional, Buck, and Boost Capability

## 2.1. Introduction

Fig. 2.1 shows that there are 4 areas to increase the performance of the DAB dc–dc converter in a large voltage variation and a wide operational range. This study only focused on the switching strategy (modulation strategy).

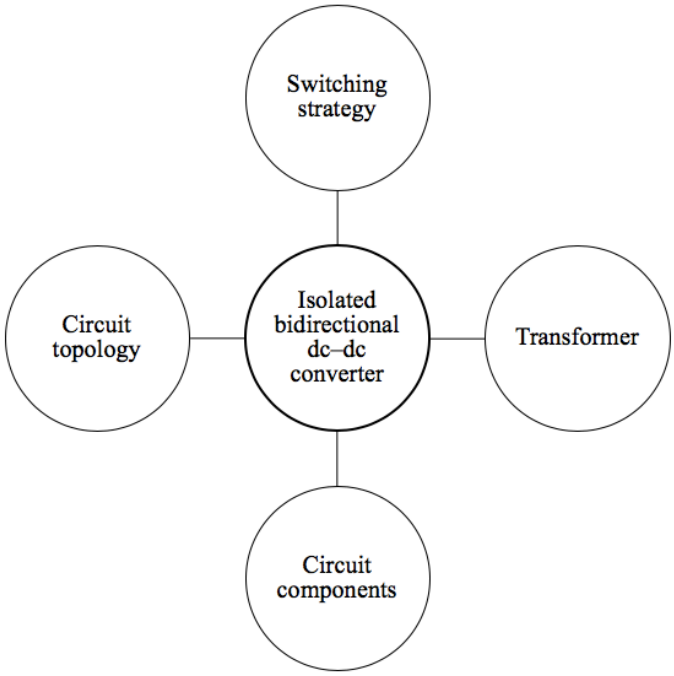



Fig. 2.1. Areas to increase the performance of the DAB dc–dc converter.

The DAB dc–dc converter has a natural soft-switching capability without additional snubber circuit [34]. However, the soft-switching operation in the DAB dc–dc converter depends on the modulation strategy. A modulation strategy is a switching pattern to control the power flow in a DAB dc–dc converter.

There are many literatures have focused on the modulation strategy to operate in a wide range of voltage variation and a wide power range. Based on these challenges, twelve suitable modulation strategies are chosen. The modulation strategies can be categorized into four categories which are one degree of

freedom, two degree of freedoms, three degrees of freedoms, and combined modulation strategy. Fig. 2.2 shows the 4 categories of the modulation strategy.

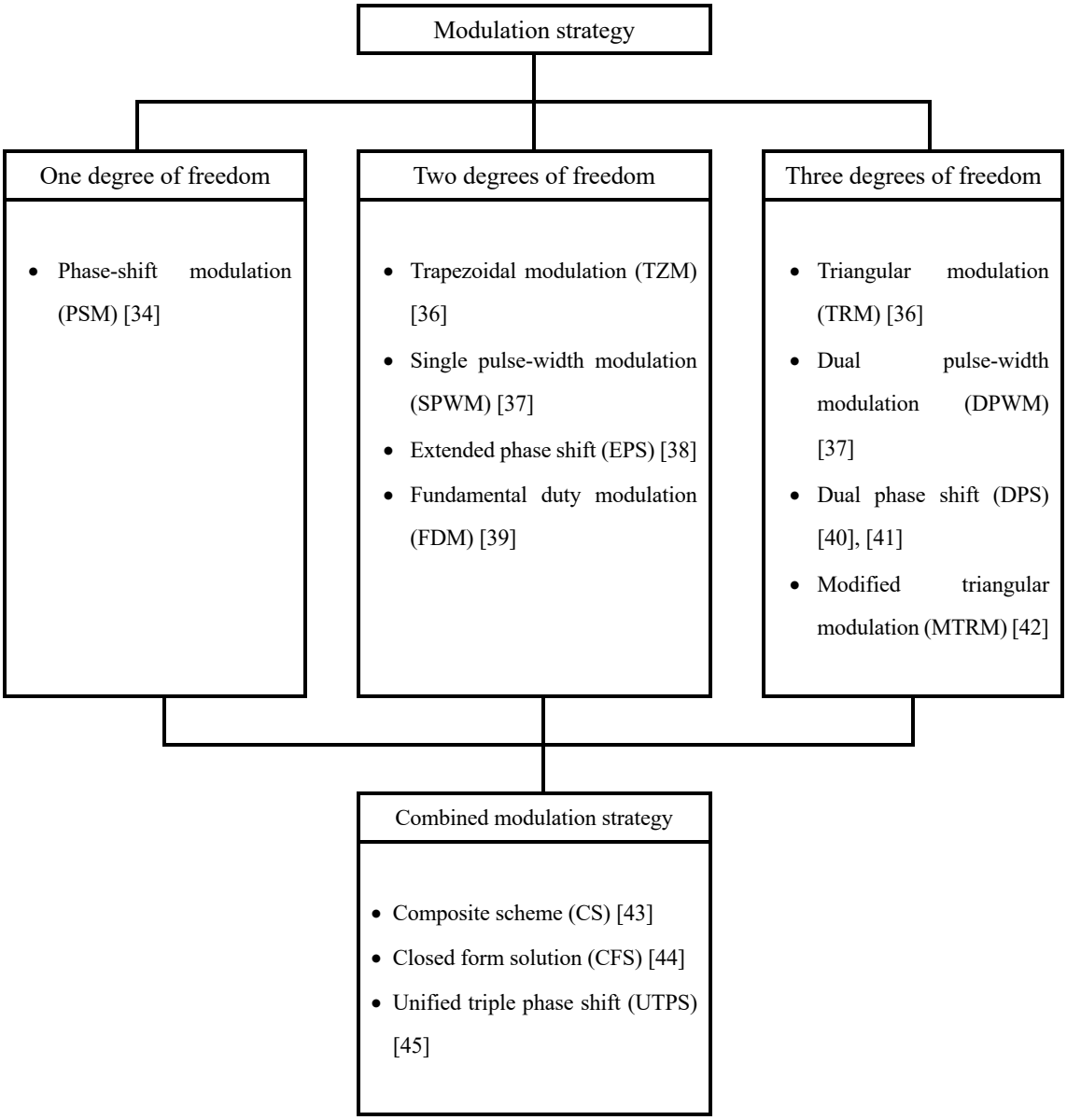



Fig. 2.2. Categories of the modulation strategy.

The first category is one degree of freedom. Only one phase is controlled in this category. Only phase-shift modulation (PSM) felt in this category. When there is a large voltage variation, PSM is not suitable due to its high circulating current and a limited soft-switching range in the low power range [34].

The second category is two degrees of freedom. Two phases are controlled in this category. Trapezoidal modulation (TZM), single pulse-width modulation (SPWM), and extended phase shift (EPS) are mostly the same modulation strategy. They are proposed to reduce the circulating current between medium to high

power transfer results in a lower RMS current than that of PSM [36]–[38]. They can also slightly extend the soft-switching range. However, they have a restricted operational range [37]. Fundamental duty modulation (FDM) operates in the low power range too and has lower circulating current than that of PSM [39]. The FDM algorithm is simple and has a wide power transfer [39]. However, the circulating current presents in the low power range and still reduces the efficiency of the DAB converter.

The modulation strategies in two degrees of freedom perform better between medium and high-power transfer. In the low power range, the modulation strategies in three degrees of freedom perform better. Especially, when there is a large voltage variation, triangular modulation (TRM) and dual pulse-width modulation (DPWM) can operate the low voltage side of the DAB converter in zero current switching (ZCS) results in lower circulating current than that of PSM, SPWM, FDM, and TZM [36]. They can extend the soft-switching operation and have a simple algorithm. However, they only operate in the low power range. Dual phase shift (DPS) can operate up to the high-power range. However, the circulating current of DPS is higher than that of PSM, SPWM, FDM, and TZM [40]. DPS is proposed to mainly reduce the startup inrush current and can bidirectional power flow [40]. Modified triangular modulation (MTRM) is also proposed to increase the operational range. However, MTRM has higher circulating current than DPS [42].

Since the modulation strategies in two and three degrees of freedom have a limited operational range, they are merged to form a combined modulation strategy [43]–[45]. The combined modulation strategy has a wider operational range, lower circulating current, and a wider soft-switching range compares to the other categories. Composite scheme reduces the circulating current over a wide power transfer with a simple algorithm. However, one degree of freedom has been neglected in the calculations [43]. Closed form solution has considered all the three degree of freedom. However, it requires extensive number of online and offline calculations [44]. Unified triple phase shift (UTPS) has considered all the three degrees of freedom and has simple algorithm. However, UTPS cannot transfer bidirectional power.

All the stated modulation strategies are lacking important qualities for the BESS. The four important qualities for the modulation strategy of the DAB converter to operate in the BESS are:

1. Simple (Processing time is below 6 μs).
2. Consider all the three degrees of freedom (Easy to be programming).
3. Bidirectional capability.
4. Wide voltage variation capability.

The comparison of the modulation strategies based on the four qualities is summarized in Table 2.1.

Table 2.1. Comparison of the modulation strategies.

| Degrees of freedom | Quality / Modulation | Simplicity | Three degrees of freedom | Bidirectional capability | Voltage variation capability | Circulating current | |
|---|---|---|---|---|---|---|---|
| | | | | | | Low to Med power range | Med to High power range |
| 1 | PSM | Simple | All is considered | Yes | $r>1$ and $r<1$ | High | High |
| 2 | SPWM/ TPM/EPS | Simple | All is considered | No | Only $r<1$ | Not possible | Low |
| | FDM | Complex | All is considered | No | Only $r<1$ | Med | Low |
| 3 | TRM/ DPWM | Simple | All is considered | No | Only r<1 | Low | Not possible |
| | DPS | Simple | All is considered | Yes | $r>1$ and $r<1$ | Low | Med |
| | MTRM | Simple | All is considered | Yes | Only $r<1$ | Med | Not possible |
| Combined | Composite Scheme | Simple | $\varphi$ is neglected | No | Only $r<1$ | Low | Low |
| | Closed form solution | Complex | All is considered | Yes | $r>1$ and $r<1$ | Low | Low |
| | UTPS | Simple | All is considered | No | Only $r<1$ | Low | Low |

## 2.2. The DAB converter

### 2.2.1. DAB converter configuration

Fig. 2.3 shows the configuration of dual active bridge (DAB) dc–dc converter. It was originally introduced in [46] and patented in [47]. It consists of primary and secondary full bridges (FB1 and FB2), a high frequency transformer with a leakage inductance, and optionally an additional series inductance $L_1$. Each power switch ($S_1$–$S_8$) has an antiparallel diode[3]. In the primary bridge, $S_1$ and $S_2$ are in leg 1, and $S_3$ and $S_4$ are in leg 2. In the secondary bridge, $S_5$ and $S_6$ are in leg 3, and $S_7$ and $S_8$ are in leg 4.

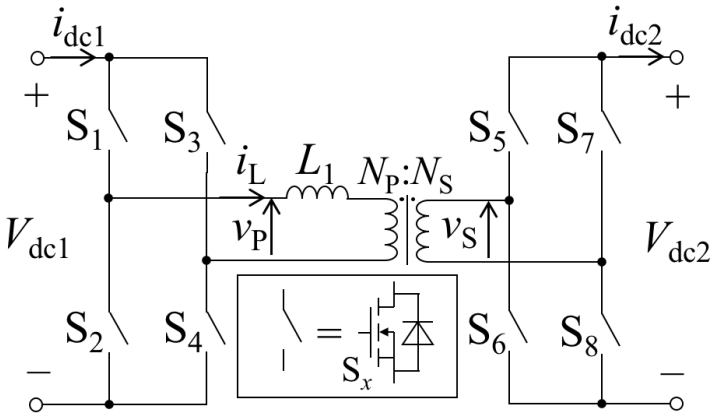



Fig. 2.3. Single phase dual active bridge dc-dc converter configuration.

Fig. 2.4 shows that the DAB converter converts from the primary dc voltage supply $V_{dc1}$ to the secondary dc voltage supply $V_{dc2}$ in three stages. The FB1 converts the primary dc voltage $V_{dc1}$ to 2 or 3 levels square ac voltage (primary square voltage $v_P$) by switching four power switches ($S_1$–$S_4$). The FB2 converts the secondary dc voltage $V_{dc2}$ to 2 or 3 levels square ac voltage (secondary square voltage $v_S$) by switching the other four switches ($S_5$–$S_8$). The primary and secondary windings of the transformer ($N_P$ and $N_S$) determine the winding ratio $n = N_P/N_S$. The voltage ratio is $r = nV_{dc2}/V_{dc1}$.

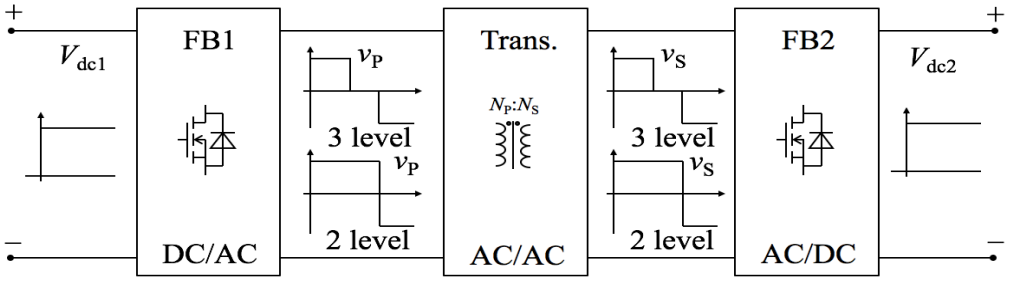



Fig. 2.4. Three stages single phase DAB dc-dc converter.

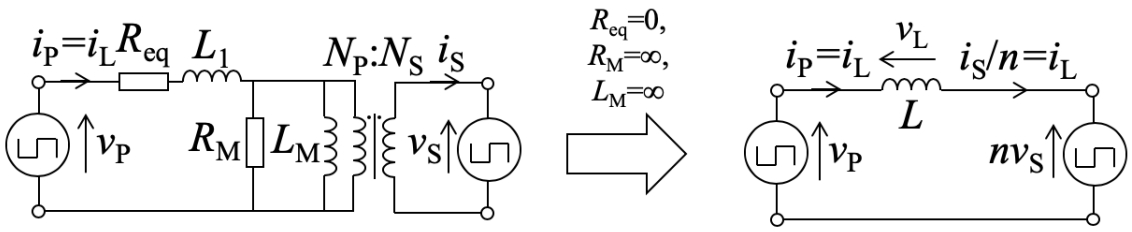
[3] The antiparallel diode can be the body diode of the power device or an external diode.

### 2.2.2. Lossless DAB converter model

In order to simplify the analysis, the DAB converter is converted to an equivalent circuit. The leakage inductance of the transformer and the additional series inductance $L_1$ can be represented as an equivalent series inductance $L$. Since the primary and secondary square voltages are ac voltage, they can be replaced as time varying primary and secondary voltages ($v_P(t)$ and $v_S(t)$). The time varying primary and secondary voltages between the series inductance $L$ results in inductance voltage $v_L$ and inductance current $i_L$. $i_P$ and $i_S$ are primary inductance current and secondary inductance current, respectively. In a lossless DAB converter circuit, the assumptions are;

1. All losses are neglected ($R_{eq}=0$, $R_M=\infty$).
2. The parasitic components are not considered.
3. The transformer magnetizing inductance is infinite ($L_M=\infty$).
4. All the components in the secondary side are referred to the primary side.
5. The primary dc voltage $V_{dc1}$ and the secondary dc voltage $V_{dc2}$ are constant.

The lossless equivalent DAB circuit is shown in Fig. 2.5(b).




(a)Practical model (b) Lossless model

Fig. 2.5. Equivalent DAB converter circuit.

In a lossless DAB converter, the primary square voltage $v_p$ and secondary square bridge $v_s$ have three possible levels in a switching period which are positive, zero, and negative value. The three levels of primary and secondary voltages with the switching states are summarized in Tables 2.2 and 2.3.

Table 2.2. Primary square voltage levels.

| | | |
|---|---|---|
| Primary square voltage $v_P(t)$ | $+V_{dc1}$ | State I : $S_1$, $S_4$ on, $S_2$, $S_3$ off |
| | 0 | State II : $S_1$, $S_3$ on, $S_2$, $S_4$ off or<br>State III : $S_2$, $S_4$ on, $S_1$, $S_3$ off |
| | $-V_{dc1}$ | State IV : $S_2$, $S_3$ on, $S_1$, $S_4$ off |

Table 2.3. Secondary square voltage levels.

| | | |
|---|---|---|
| Secondary square voltage $v_S(t)$ | $+V_{dc2}$ | State I : $S_5$, $S_8$ on, $S_6$, $S_7$ off |
| | 0 | State II : $S_5$, $S_7$ on, $S_6$, $S_8$ off or<br>State III : $S_6$, $S_8$ on, $S_5$, $S_7$ off |
| | $-V_{dc2}$ | State IV : $S_6$, $S_7$ on, $S_5$, $S_8$ off |

The inductance voltage $v_L(t)$ between the series inductance $L$ becomes

$$v_L(t) = v_P(t) - v_S(t). \tag{2.1}$$

When the inductance voltage in (2.1) is applied to the transformer, the current starts to flow in the transformer. The current is the inductance current $i_L$ in the equivalent DAB circuit. The inductance current is calculated with,

$$i_L(t_1) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t_1} v_L(t)\,dt, \tag{2.2}$$

where $t_0<t_1$, $i_L(t_0)$ is the initial inductance current at time $t_0$, and $i_L(t_1)$ is the inductance current at time $t_1$. When the inductance current is multiplied with the primary square voltage $v_P$ or the secondary square voltage $v_S$, the instantaneous power at primary and secondary side are,

$$p_P(t) = v_P(t) \times i_P(t), \tag{2.3}$$

and

$$p_S(t) = nv_S(t) \times i_P(t), \tag{2.4}$$

respectively. To simplify the inductance current in (2.2), the time interval between $t_0$ to $t_1$ is selected during $v_P(t)$ and $v_S(t)$ are constant.

Then, the average power over the switching period $T_S$ is calculated with,

$$P_P = \frac{1}{T_S}\int_{t_0}^{t_0+T_S} p_P(t)\,dt, \tag{2.5}$$

for the primary side and

$$P_S = \frac{1}{T_S}\int_{t_0}^{t_0+T_S} p_S(t)\,dt, \tag{2.6}$$

for the secondary side. In one switching period, there are several intervals to express the 2 or 3 levels of the primary square voltage $v_P$ and the secondary square voltage $v_S$. Therefore, one switching period is split up to $m$ time intervals,

$$\begin{aligned} &\text{time interval 1 :} && t_0 < t < t_1, \\ &\text{time interval 2 :} && t_1 < t < t_2, \\ &\quad\vdots \\ &\text{time interval } m\text{ :} && t_{m-1} < t < t_m = t_0 + T_S. \end{aligned} \tag{2.7}$$

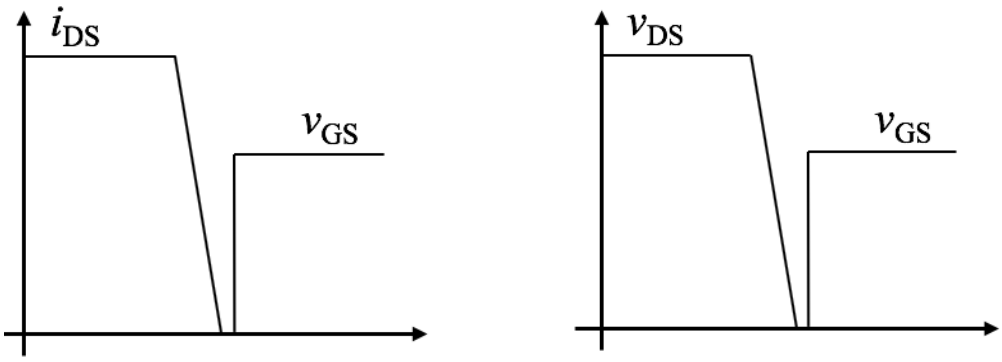
According to (2.3), (2.4), (2.5), and (2.6), the primary $v_P(t)$ and secondary $v_S(t)$ square voltages determine the primary and secondary power,

$$P_P = P_S \tag{2.8}$$

The above equation is only applicable in a lossless DAB converter. From this section, the power transfer also depends on the switching frequency, the series inductance $L$, and the square voltages $v_P$ and $v_S$ that are applied to the transformer.

### 2.2.3. Soft-switching in DAB converter

Fig. 2.6 shows that there are two types of soft-switching, zero current switching (ZCS) and zero voltage switching (ZVS). In ZCS, each power device is turned on or turned off when the current through drain and source is zero (Fig. 2.6 (a)). In ZVS, each power device is turned on or turned off when the voltage between drain and source is zero (Fig. 2.6 (b)). The soft-switching operation reduces the switching losses.




(a) (b)

Fig. 2.6. Types of soft-switching. (a) ZCS, (b) ZVS.

## 2.3. Modulation strategy analysis

A combined modulation strategy is needed to transfer power in a wide operational range and a wide power transfer. Most of the combined modulation strategies consist of SPWM and DPWM [43]–[45]. In this section, SPWM and DPWM are analyzed.

### 2.3.1. Modulation strategy

Fig. 2.7 shows a conventional open-loop controller where the power transfer $P_o$ is regulated with one controllable parameter (fundamental phase $\varphi_f$). Modulation strategy regulates the primary square voltage and the secondary square voltage. Basically, the square voltages $v_P$ and $v_S$ depend on the three degrees of freedom which are the phase $\varphi$, the primary voltage width $\tau_P$, and the secondary voltage width $\tau_S$. The three degrees of freedom ($\varphi$, $\tau_P$, $\tau_S$) can be combined into the fundamental phase $\varphi_f$. The relation between the fundamental phase $\varphi_f$ and the three degrees of freedom is

$$\varphi_{\mathrm{f}} = \varphi + \frac{\tau_{\mathrm{S}} - \tau_{\mathrm{P}}}{2}. \tag{2.9}$$

When $\varphi_{\mathrm{f}} > 0$, the power is transferred from the primary voltage to the secondary voltage ($V_{\mathrm{dc1}}$ to $V_{\mathrm{dc2}}$). When $\varphi_{\mathrm{f}} < 0$, the power is transferred from the secondary voltage $V_{\mathrm{dc2}}$ to the primary voltage $V_{\mathrm{dc1}}$. Then, the pulse-width modulation (PWM) generator depicts that the switching patterns of each power devices ($S_1$-$S_8$) depends on the three degrees of freedom.

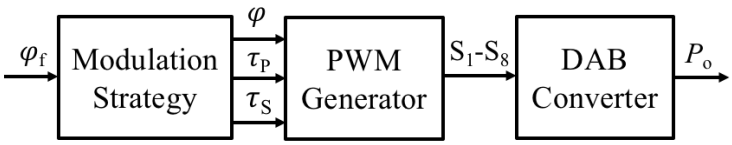



Fig. 2.7. Open-loop controller.

Fig. 2.8 shows waveforms of a modulation strategy with the switching patterns of each power devices ($S_1$-$S_8$). The power devices are assumed to operate in an ideal manner. The phase $\varphi$ is the phase between leg 1 ($S_1$, $S_2$) and leg 3 ($S_5$, $S_6$). The primary voltage width $\tau_{\mathrm{P}}$ is the phase between leg 1 and leg 2 ($S_3$, $S_4$). The secondary voltage width $\tau_{\mathrm{S}}$ is the phase between leg 3 and leg 4 ($S_7$, $S_8$). The duty cycle of the PWM waveforms are always 0.5 without considering the dead time. In a leg (leg 1, leg 2, leg 3, or leg 4), the

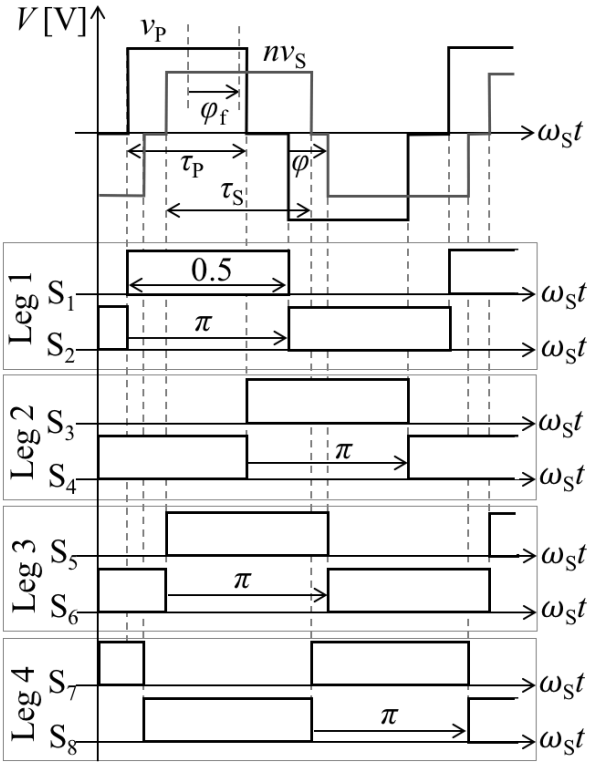



Fig. 2.8. Waveforms of a modulation strategy with the switching patterns of each power devices.

phase between upper and lower power devices are always π [rad]. Shifting the three degrees of freedom ($\varphi$, $\tau_P$, $\tau_S$) defines the type of the modulation strategy.

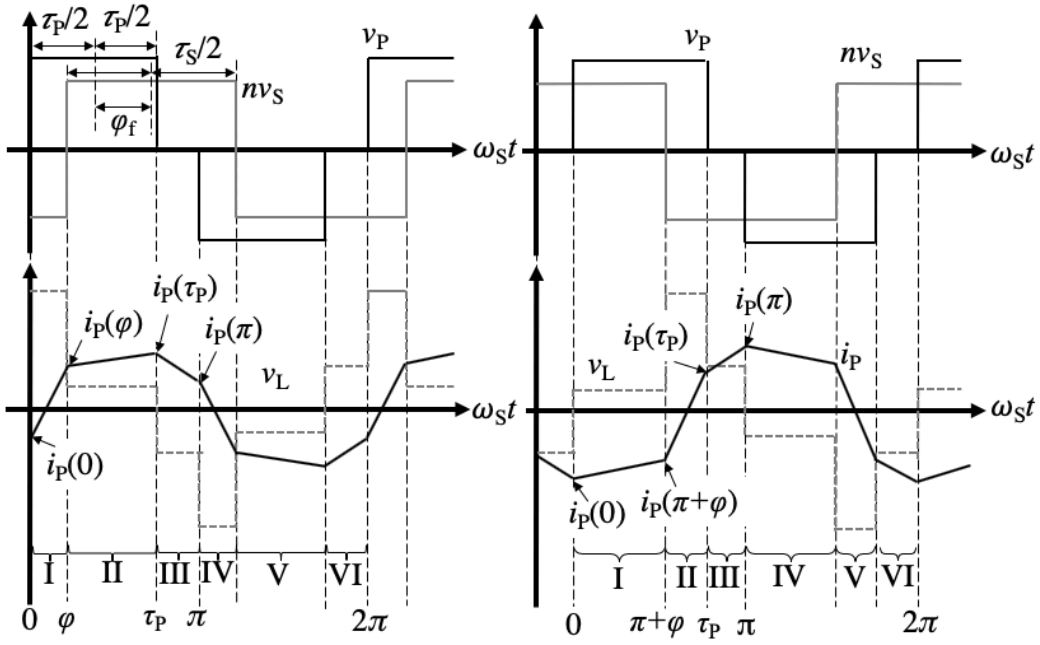
### 2.3.2. Single pulse-width modulation

When the voltage ratio is less than one $r$<1, single pulse-width modulation (SPWM) is a strategy that controls the phase $\varphi$ and the primary voltage width $\tau_P$, and fixes the secondary voltage width $\tau_S$ to π [rad]. The voltage width of the lower voltage side is always fixed to π. Hence, from Tables 2.2 and 2.3, there are states I, II, III and IV in primary square voltage, and states I and IV in secondary square voltage. Fig. 2.9 shows a steady-state condition of the SPWM waveforms when the voltage ratio is less than one ($r$ < 1). The voltages $v_P(t)$ and $v_S(t)$ and the primary current $i_P(t)$ repeat every full cycle $T_S$. The second half cycle has the negative value of the first half cycle:

$$v_P(t) = -v_P\left(t + \frac{T_S}{2}\right),$$

$$nv_S(t) = -nv_S\left(t + \frac{T_S}{2}\right), \text{and} \tag{2.10}$$

$$i_P(t) = -i_P\left(t + \frac{T_S}{2}\right).$$




(a) (b)

Fig. 2.9. The single pulse-width modulation waveforms
during (a) positive power transfer. (b) negative power transfer.

The primary voltage $V_{dc1}$ and the secondary voltage $V_{dc2}$ are constant during the first and the second half cycle (time intervals I, II, III, and IV in Fig. 2.9). Since the waveform is repeated every half cycle, only the first half cycle is needed to calculate the power transfer. The primary power transfer from (2.3) and (2.5) is,

$$\begin{aligned} P_{\mathrm{P}} &= \frac{1}{T_{\mathrm{S}}}\int_0^{T_{\mathrm{S}}} p_{\mathrm{P}}(t)\,dt = \frac{2}{T_{\mathrm{S}}}\int_0^{T_{\mathrm{S}}/2} v_{\mathrm{P}}(t) i_{\mathrm{P}}(t)\,dt \\ &= \frac{2V_{\mathrm{dc1}}}{T_{\mathrm{S}}}\int_0^{T_{\mathrm{S}}/2} i_{\mathrm{P}}(t)\,dt. \end{aligned} \tag{2.11}$$

The primary inductance current is needed to calculate the power transfer. The relationship between the time interval and the phase is $t=\theta/\omega_{\mathrm{S}}$. From (2.2), (2.7), time intervals I, II, and III ($0 < t < T_{\mathrm{S}}/2$) in Fig. 2.9(a), the primary inductance current in the positive power transfer can be expressed as:

$$\text{time interval I } \left(0 \le t \le \frac{\varphi}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}(0) + \frac{V_{\mathrm{dc1}} + nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}} L}\varphi \tag{2.12}$$

$$\text{time interval II } \left(\frac{\varphi}{\omega_{\mathrm{S}}} \le t \le \frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) + \frac{V_{\mathrm{dc1}} - nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}} L}(\tau_{\mathrm{P}} - \varphi) \tag{2.13}$$

$$\text{time interval III } \left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}} \le t \le \frac{\pi}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\pi}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) - \frac{nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}} L}(\pi - \tau_{\mathrm{P}}) \tag{2.14}$$

$$i_{\mathrm{P}}(0) = -i_{\mathrm{P}}\left(\frac{\pi}{\omega_{\mathrm{S}}}\right). \tag{2.15}$$

From (2.12), (2.13), (2.14), (2.15), and $\omega_{\mathrm{S}}=2\pi f_{\mathrm{S}}$, the leakage inductance current at 0 is

$$i_{\mathrm{P}}(0) = \frac{nV_{\mathrm{dc2}}(\pi - 2\varphi) - V_{\mathrm{dc1}}\tau_{\mathrm{P}}}{2\omega_{\mathrm{S}} L} \tag{2.16}$$

From (2.11), (2.12), (2.13), (2.14), (2.15), (2.16), and considering the positive range $0 < \varphi_{\mathrm{f}} < \pi/2$, the power transfer is

$$P = P_{\mathrm{P}} = P_{\mathrm{S}} = \frac{nV_{\mathrm{dc1}}V_{\mathrm{dc2}}}{4\pi^2 f_{\mathrm{S}} L}(2\varphi\tau_{\mathrm{P}} - 2\varphi^2 - {\tau_{\mathrm{P}}}^2 + \tau_{\mathrm{P}}\pi).\ \forall\varphi > 0 \tag{2.17}$$

The power transfer depends on the primary voltage width and the phase. This shows that SPWM can transfer medium power transfer with the same fundamental phase by reducing the primary voltage width. This modulation is not widely used because the direction of power transfer does not correspond fully to the positive and negative value of $\varphi$. Actually, the power transfer depends on the fundamental phase $\varphi_{\mathrm{f}}$ [48]. In SPWM, when the fundamental phase is;

$$\begin{aligned} &\varphi_{\mathrm{f}} > 0 : \text{the power is transferred from the primary to the secondary bridge,} \\ &\varphi_{\mathrm{f}} < 0 : \text{the power is transferred from the secondary to the primary bridge,} \end{aligned} \tag{2.18}$$

where the fundamental phase shift of SPWM is

$$\varphi_{\mathrm{f}} = \varphi + \frac{\pi - \tau_{\mathrm{P}}}{2}. \tag{2.19}$$

In the positive power transfer, the soft-switching operation is achieved for all power devices when the leakage current conditions are;

$$i_{\mathrm{P}}(0) \leq 0 \text{ for Leg 1,} \tag{2.20}$$

$$i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) \geq 0 \text{ for Leg 2,} \tag{2.21}$$

$$i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) \geq 0 \text{ for Leg 3,} \tag{2.22}$$

$$i_{\mathrm{P}}\left(\frac{\pi+\varphi}{\omega_{\mathrm{S}}}\right) \leq 0 \text{ for Leg 4.} \tag{2.23}$$

In SPWM, when $r$<1, the hard-switching only occurs in the leg 3 and leg 4 [49]. From (2.10), leg 4 operates in soft-switching when leg 3 is operating in soft-switching. From (2.12), (2.16), and (2.22), the soft-switching boundary of SPWM is

$$\varphi \geq \frac{\pi}{2}\left(\frac{\tau_{\mathrm{P}}}{\pi} - r\right), \tag{2.24}$$

The converter operates in the ZVS starting from $\varphi$>0 if the primary voltage width is $\tau_{\mathrm{P}}= \pi r$. In order to match $\varphi$ of SPWM with that of PSM, the phase is expressed using the fundamental phase by using (2.19). The value of phase in (2.19) is inserted into (2.24), the soft-switching boundary in fundamental phase is given by

$$\varphi_{\mathrm{f}} \geq \frac{\pi}{2}(1-r), \tag{2.25}$$

This shows that as long as the fundamental phase satisfies (2.25) during the positive power transfer, SPWM operates in the soft-switching. The soft-switching range of SPWM is equal to that of PSM based on the fundamental value. However, the power transfer is lower when the primary voltage width is lower. When the voltage ratio $r$ is 0.5, the soft-switching range increases up to 33% compared to PSM [48].

From (2.2), (2.7), time intervals I, II, and III ($0 < t < T_{\mathrm{S}}/2$) in Fig. 2.9(b), the primary inductance current in the negative power transfer can be expressed as:

$$\text{time interval I } \left(0 \leq t \leq \frac{\pi+\varphi}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}(0) + \frac{V_{\mathrm{dc1}} - nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}}L}(\pi+\varphi) \tag{2.26}$$

$$\begin{aligned}\text{time interval II } \left(\frac{\pi+\varphi}{\omega_{\mathrm{S}}} \leq t \leq \frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right):\ & i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) \\ & = i_{\mathrm{P}}\left(\frac{\pi+\varphi}{\omega_{\mathrm{S}}}\right) + \frac{V_{\mathrm{dc1}} + nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}}L}(\tau_{\mathrm{P}} - \pi - \varphi)\end{aligned} \tag{2.27}$$

$$\text{time interval III } \left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}} \leq t \leq \frac{\pi}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\pi}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) + \frac{nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}}L}(\pi - \tau_{\mathrm{P}}) \tag{2.28}$$

$$i_{\mathrm{P}}(0) = -i_{\mathrm{P}}\left(\frac{\pi}{\omega_{\mathrm{S}}}\right). \tag{2.29}$$

From (2.26), (2.27), (2.28), (2.29), and $\omega_S=2\pi f_S$, the leakage inductance current at 0 is

$$i_P(0) = \frac{nV_{dc2}(\pi + 2\varphi) - V_{dc1}\tau_P}{2\omega_S L} \tag{2.30}$$

In the negative power transfer, the soft-switching operation is achieved for all power devices when the leakage current conditions are;

$$i_P(0) \leq 0 \text{ for Leg 1,} \tag{2.31}$$

$$i_P\left(\frac{\tau_P}{\omega_S}\right) \geq 0 \text{ for Leg 2,} \tag{2.32}$$

$$i_P\left(\frac{\varphi}{\omega_S}\right) \geq 0 \text{ for Leg 3,} \tag{2.33}$$

$$i_P\left(\frac{\pi + \varphi}{\omega_S}\right) \leq 0 \text{ for Leg 4.} \tag{2.34}$$

In SPWM, when $r<1$, the hard-switching only occurs in the leg 3 and leg 4 [49]. From (2.29), leg 4 operates in soft-switching when leg 3 is operating in soft-switching. From (2.26), (2.30), and (2.34), the soft-switching boundary of SPWM is

$$\varphi \leq \frac{1}{2}(r\pi - 2\pi + \tau_P), \tag{2.35}$$

In order to match $\varphi$ of SPWM with that of PSM, the phase is expressed using the fundamental phase by using (2.19). The value of phase from (2.19) is inserted into (2.35), the soft-switching boundary in fundamental phase is given by

$$\varphi_f \leq -\frac{\pi}{2}(1 - r), \tag{2.36}$$

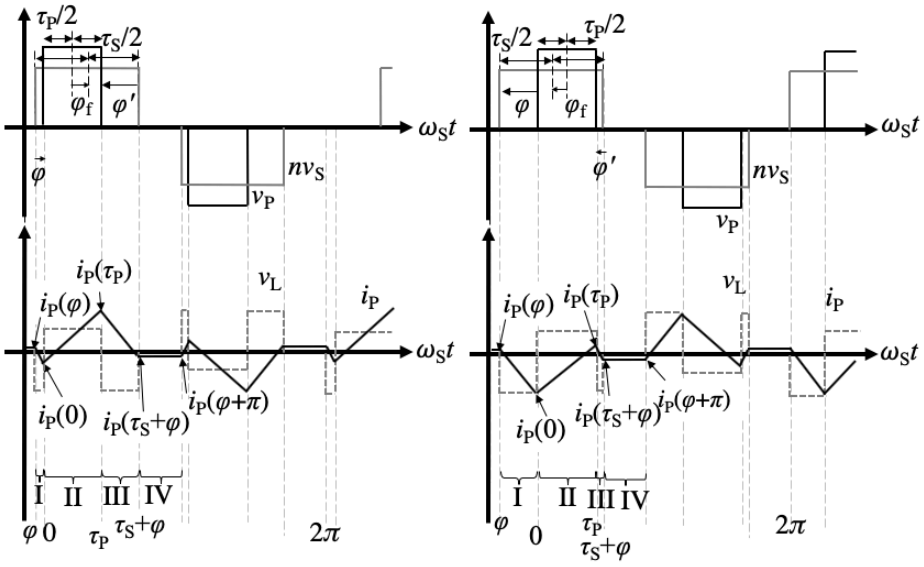
This shows that as long as the fundamental phase satisfies (2.36) during the negative power transfer, SPWM operates in the soft-switching.

### 2.3.3. Dual pulse-width modulation

Dual pulse-width modulation (DPWM) or triangular modulation (TRM) is an algorithm that controls the phase $\varphi$, the primary voltage width $\tau_P$, and the secondary voltage width $\tau_S$. From Tables 2.2 and 2.3, there are states I, II, III and IV in primary square voltage and secondary square voltage. Fig. 2.10 shows a steady-state condition of dual pulse-width modulation waveforms where the voltages $v_P(t)$ and $v_S(t)$ and the leakage inductance current $i_P(t)$ repeat every full cycle $T_S$. Traditionally, in the negative power transfer, the phase is expressed in terms of the inverse phase $\varphi'$ defined by

$$\varphi' = \tau_S - \tau_P + \varphi. \tag{2.37}$$

The inverse phase is the phase between legs 2 and 4. In this work, the phase $\varphi$ for positive and negative is always the phase between legs 1 and 3. This means the phase $\varphi$ and the fundamental phase $\varphi_f$ have positive and negative values, which enables the bidirectional power transfer. In a steady state, (2.10) is applicable for DPWM too.




(a) (b)

Fig. 2.10. The dual pulse-width modulation waveforms
during (a) positive power transfer. (b) negative power transfer.

From (2.2), (2.7), time intervals I, II, III, and IV ($0 < t < T_S/2$) in Fig. 2.10(a) and (b), the primary inductance current in the positive and negative power transfer can be expressed as:

$$\text{time interval I } \left(\frac{\varphi}{\omega_S} \le t \le 0\right): \; i_P(0) = i_P\left(\frac{\varphi}{\omega_S}\right) + \frac{nV_{dc2}}{\omega_S L}\varphi \tag{2.38}$$

$$\text{time interval II } \left(0 \le t \le \frac{\tau_P}{\omega_S}\right): \; i_P\left(\frac{\tau_P}{\omega_S}\right) = i_P(0) + \frac{V_{dc1} - nV_{dc2}}{\omega_S L}\tau_P \tag{2.39}$$

$$\text{time interval III } \left(\frac{\tau_P}{\omega_S} \le t \le \frac{\tau_S + \varphi}{\omega_S}\right): \; i_P\left(\frac{\tau_S + \varphi}{\omega_S}\right) = i_P\left(\frac{\tau_P}{\omega_S}\right) - \frac{nV_{dc2}}{\omega_S L}(\tau_S + \varphi - \tau_P) \tag{2.40}$$

$$i_P\left(\frac{\varphi}{\omega_S}\right) = -i_P\left(\frac{\tau_S + \varphi}{\omega_S}\right). \tag{2.41}$$

From (2.38), (2.39), (2.40), (2.41), and $\omega_S = 2\pi f_S$, the leakage inductance current at $\varphi$ is

$$i_P\left(\frac{\varphi}{\omega_S}\right) = \frac{nV_{dc2}\tau_S - V_{dc1}\tau_P}{2\omega_S L} \tag{2.42}$$

From (2.11), (2.38), (2.39), (2.40), (2.41), (2.42), and considering the full power range $-\pi/2 < \varphi_f < \pi/2$, the power transfer is

$$P = P_P = P_S = \frac{nV_{dc1}V_{dc2}}{4\pi^2 f_S L}(2\varphi\tau_P - {\tau_P}^2 + \tau_P\tau_S). \tag{2.43}$$

The power transfer depends on the phase, the primary and secondary voltage widths. This shows that DPWM can transfer low power transfer by reducing the primary and secondary voltage widths.

In the positive power transfer (Fig. 2.10(a)), the soft-switching operation is achieved for all power devices when the leakage current conditions are (noted that some points operates in ZCS [48]);

$$i_{\mathrm{P}}(0) = 0 \text{ for Leg 1,} \tag{2.44}$$

$$i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) \geq 0 \text{ for Leg 2,} \tag{2.45}$$

$$i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) = 0 \text{ for Leg 3,} \tag{2.46}$$

$$i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{S}} + \varphi}{\omega_{\mathrm{S}}}\right) = 0 \text{ for Leg 4.} \tag{2.47}$$

From (2.38), (2.44), and (2.46), DPWM operates in the ZCS at positive power transfer if

$$\varphi = 0. \tag{2.48}$$

From (2.42), and (2.46), the ZCS boundary for legs 3 and 4 is

$$\tau_{\mathrm{P}} = r\tau_{\mathrm{S}}. \tag{2.49}$$

From (2.9), (2.48), and (2.49), the soft-switching boundary in fundamental phase is given by

$$\varphi_{\mathrm{f}} = \frac{\tau_{\mathrm{S}}}{2}(1 - r). \tag{2.50}$$

Since the limit of the secondary voltage width of DPWM is π, the maximum fundamental phase of DPWM during positive power is

$$\varphi_{\mathrm{f\_max}} = \frac{\pi}{2}(1 - r). \tag{2.51}$$

In the negative power transfer (Fig. 2.10(b)), the soft-switching operation is achieved for all power devices when the leakage current conditions are (noted that some points operates in ZCS [48]);

$$i_{\mathrm{P}}(0) \leq 0 \text{ for Leg 1,} \tag{2.52}$$

$$i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) = 0 \text{ for Leg 2,} \tag{2.53}$$

$$i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) = 0 \text{ for Leg 3,} \tag{2.54}$$

$$i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{S}} + \varphi}{\omega_{\mathrm{S}}}\right) = 0 \text{ for Leg 4.} \tag{2.55}$$

From (2.40), (2.53), and (2.55), DPWM operates in the ZCS at negative power transfer if

$$\varphi = \tau_{\mathrm{P}} - \tau_{\mathrm{S}}. \tag{2.56}$$

From (2.42), and (2.54), the ZCS boundary for leg 3 and leg 4 is

$$\tau_{\mathrm{P}} = r\tau_{\mathrm{S}}. \tag{2.57}$$

From (2.9), (2.56), and (2.57), the soft-switching boundary in fundamental phase is given by

$$\varphi_{\mathrm{f}} = -\frac{\tau_{\mathrm{S}}}{2}(1 - r). \tag{2.58}$$

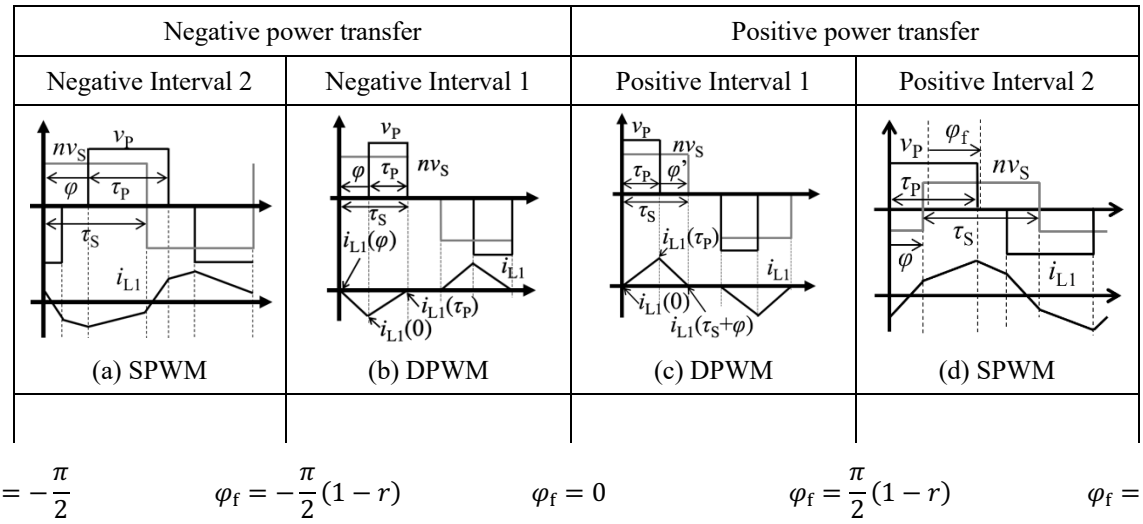



Fig. 2.11. The combined pulse-width modulation waveforms.

Since the limit of the secondary voltage width of DPWM is π, the maximum fundamental phase of DPWM during negative power is

$$\varphi_{f\_max} = -\frac{\pi}{2}(1-r). \tag{2.59}$$

# 2.4. Combined pulse-width modulation (CPWM)

In this section, the SPWM and DPWM are combined to include all three degrees of freedom and to enable bidirectional capability. The proposed modulation strategy is named combined pulse-width modulation (CPWM). The algorithm of CPWM combines the three degrees of freedom ($\varphi$, $\tau_P$, $\tau_S$) into the fundamental phase $\varphi_f$ and the voltage ratio $r$. The waveform transition of CPWM is shown in Fig. 2.11.

## 2.4.1. Fundamental phase interval classification

The first interval is for low to medium power transfer and the second interval is for medium to high power transfer. Both intervals are defined for the smooth transition, the wide operational range, and the bidirectional capability.

The boundary between the first and second interval depends on the maximum soft-switching range of DPWM in (2.51) and (2.59), and the soft-switching range of SPWM in (2.25) and (2.36). The positive boundary between the first and second interval is

$$\varphi_f = \frac{\pi}{2}(1-r). \tag{2.60}$$

The negative boundary between the first and second interval is

$$\varphi_f = -\frac{\pi}{2}(1-r). \tag{2.61}$$

The fundamental phase range for negative and positive Interval 1 is

$$\text{Interval 1}: -\frac{\pi}{2}(1-r) < \varphi_{\mathrm{f}} < \frac{\pi}{2}(1-r). \tag{2.62}$$

The fundamental phase range for negative and positive Interval 2 is

$$\text{Interval 2}: \begin{matrix} -\frac{\pi}{2} \le \varphi_{\mathrm{f}} \le -\frac{\pi}{2}(1-r). \\ \frac{\pi}{2}(1-r) \le \varphi_{\mathrm{f}} \le \frac{\pi}{2}. \end{matrix} \tag{2.63}$$

In these interval classifications, the three degrees of freedom are calculated accordingly.

### 2.4.2. Interval 1 algorithm

In order to maintain the soft-switching in the positive Interval 1, the three degrees of freedom are calculated based on the soft-switching conditions in (2.48) and (2.49). From (2.9), (2.48), and (2.49), the phase is

$$\varphi = 0, \tag{2.64}$$

and the secondary voltage width is

$$\tau_{\mathrm{S}} = \frac{2}{1-r}\varphi_{\mathrm{f}}. \tag{2.65}$$

From (2.49) and (2.65), the primary voltage width is

$$\tau_{\mathrm{P}} = \frac{2r}{1-r}\varphi_{\mathrm{f}}. \tag{2.66}$$

In order to maintain the soft-switching in the negative Interval 1, the three degrees of freedom are calculated based on the soft-switching conditions in (2.56) and (2.57). From (2.9) and (2.56), the phase is

$$\varphi = 2\varphi_{\mathrm{f}}, \tag{2.67}$$

From (2.9), (2.57), (2.67), the secondary voltage width is

$$\tau_{\mathrm{S}} = -\frac{2}{1-r}\varphi_{\mathrm{f}}. \tag{2.68}$$

From (2.57), (2.68), the primary voltage width is

$$\tau_{\mathrm{P}} = -\frac{2r}{1-r}\varphi_{\mathrm{f}}. \tag{2.69}$$

For the positive and negative Interval 1, the positive {(2.64), (2.65), (2.66)} and negative {(2.67), (2.68), (2.69)} three degrees of freedom are combined into

$$\varphi = \varphi_{\mathrm{f}} - |\varphi_{\mathrm{f}}|, \tag{2.70}$$

$$\tau_{\mathrm{S}} = \frac{2}{1-r}|\varphi_{\mathrm{f}}|, \tag{2.71}$$

$$\tau_{\mathrm{P}} = \frac{2r}{1-r}|\varphi_{\mathrm{f}}|. \tag{2.72}$$

When the fundamental phase and the secondary voltage width reach $\pm\pi(1-r)/2$ and $\pi$, respectively, DPWM has reached its operational limit. SPWM is needed to increase the power range.

### 2.4.3. Interval 2 algorithm

To extend the power range in the positive Interval 2, the primary voltage width is gradually changed from $\tau_P = r\pi$ at the boundary of Interval 1 and Interval 2 $\{\varphi_f=\pi(1-r)/2\}$ to $\tau_P = \pi$ at the maximum fundamental phase $\varphi_f=\pi/2$. The secondary voltage width is fixed to $\pi$. The linear variation and gradient comparison of the primary voltage width with the fundamental phase, which is the simplest method, yields

$$\tau_P = \frac{(1-r)}{r}(2\varphi_f - \pi) + \pi. \tag{2.73}$$

From (2.19), (2.73), and $\tau_S = \pi$, the phase is

$$\varphi = \varphi_f + \frac{(1-r)}{2r}(2\varphi_f - \pi). \tag{2.74}$$

To extend the power range in the negative Interval 2, the primary voltage width is gradually changed from $\tau_P = r\pi$ at the boundary of Interval 1 and Interval 2 $\{\varphi_f=-\pi(1-r)/2\}$ to $\tau_P = \pi$ at the maximum fundamental phase $\{\varphi_f=-\pi/2\}$. The secondary voltage width is fixed to $\pi$. The linear variation and gradient comparison of the primary voltage width with the fundamental phase, which is the simplest method, yields

$$\tau_P = \frac{(1-r)}{r}(-2\varphi_f - \pi) + \pi. \tag{2.75}$$

From (2.19), (2.75), and $\tau_S = \pi$, the phase is

$$\varphi = \varphi_f + \frac{(1-r)}{2r}(-2\varphi_f - \pi). \tag{2.76}$$

For the positive and negative Interval 2, the positive {(2.73), (2.74)} and negative {(2.75), (2.76)} equations of the three degrees of freedom are combined into

$$\varphi = \varphi_f + \frac{(1-r)}{2r}(2|\varphi_f| - \pi), \tag{2.77}$$

$$\tau_S = \pi, \tag{2.78}$$

$$\tau_P = \frac{(1-r)}{r}(2|\varphi_f| - \pi) + \pi. \tag{2.79}$$

### 2.4.4. Boost ($r$>1) algorithm

In this case when the secondary voltage rises, which the voltage ratio becomes more than one, the algorithm of CPWM is slightly different from that of $r$<1. The inverse voltage ratio is used instead of the voltage ratio, which is defined by

$$r' = \frac{1}{r} = \frac{V_{dc1}}{nV_{dc2}}. \tag{2.80}$$

In this condition, the secondary voltage width is reduced in Interval 2 and the primary voltage width must be larger than the secondary voltage width in Interval 1. For the positive and negative Interval 1, the three degrees of freedom become

$$\varphi = \varphi_{\mathrm{f}} + |\varphi_{\mathrm{f}}|, \tag{2.81}$$

$$\tau_{\mathrm{P}} = \frac{2}{1-r'}|\varphi_{\mathrm{f}}|, \tag{2.82}$$

$$\tau_{\mathrm{S}} = \frac{2r'}{1-r'}|\varphi_{\mathrm{f}}|. \tag{2.83}$$

For the positive and negative Interval 2, the three degrees of freedom become

$$\varphi = \varphi_{\mathrm{f}} - \frac{(1-r')}{2r'}(2|\varphi_{\mathrm{f}}| - \pi), \tag{2.84}$$

$$\tau_{\mathrm{P}} = \pi, \tag{2.85}$$

$$\tau_{\mathrm{S}} = \frac{(1-r')}{r'}(2|\varphi_{\mathrm{f}}| - \pi) + \pi. \tag{2.86}$$

The algorithm of CPWM is summarized in Fig. 2.12. Fig. 2.13 is the peak current varied with power transfer of PSM and that of CPWM when voltage ratio $r$=0.5. The straight line represents PSM. The dashed line represents CPWM. CPWM has an overall lower peak current than PSM.

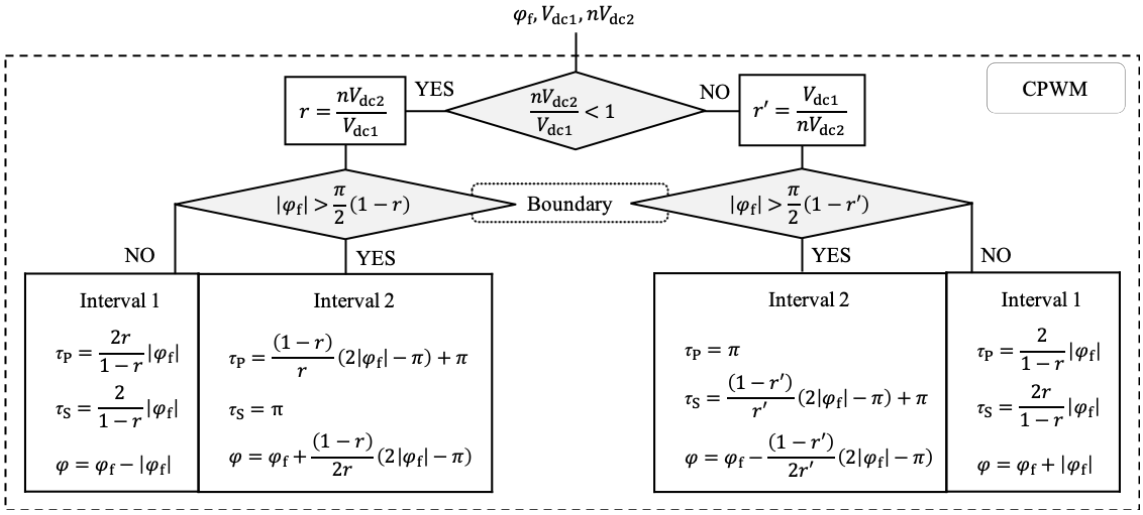


Fig. 2.12. The CPWM algorithm.

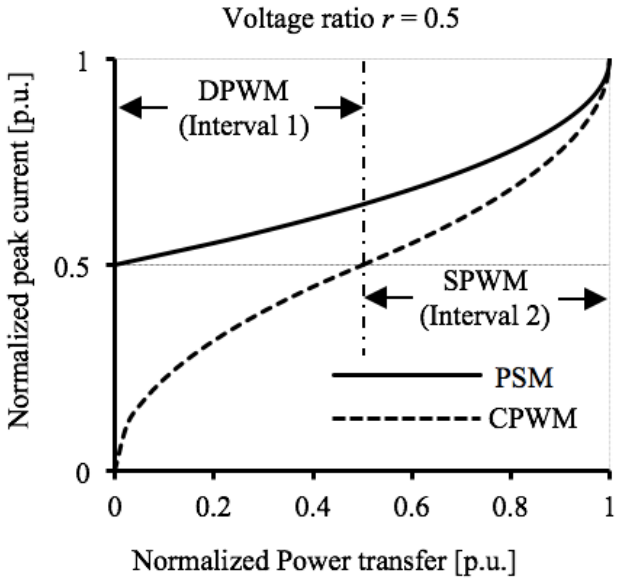



Fig. 2.13. Normalized peak current varied with normalized power transfer of CPWM and that of PSM [49].

## 2.5. Experiment

CPWM are experimented with the first prototype in this section to validate the power transfer and soft-switching operation in a voltage variation condition. The voltage ratio $r$=0.5 is chosen to operate the converter in an unfavorable voltage variation scenario while the convenient condition is $r$=1. Furthermore, the efficiency of PSM and CPWM are compared.

### 2.5.1. Experimental parameters

The first prototype of the DAB converter is designed, and the configuration is shown in Fig. 2.14. The primary and secondary voltages are fixed at 380 V. The total leakage inductance is 62 μH. The core of the transformer is a toroidal core (FINEMET, Hitachi Metals). The primary to secondary winding ratio is 1:2. In this case, the voltage ratio $r$ becomes 0.5. The dead time is fixed at 0.24 μs. The switching frequency is 80 kHz. All the power devices are SiC MOSFETs (SCH2080KE, ROHM). The parameters of the first prototype are summarized in Table 2.4.

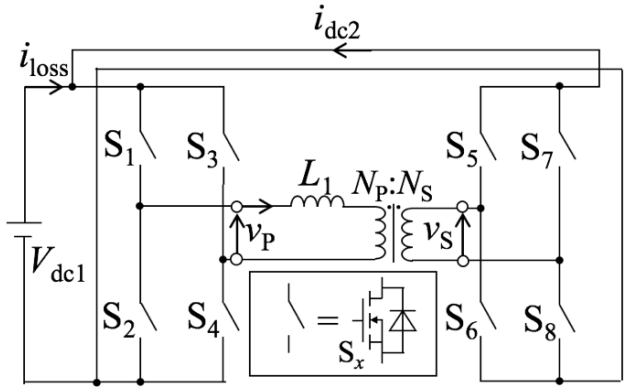



Fig. 2.14. DAB converter configuration.

Table 2.4. Parameters of the first prototype.

| | |
|---|---|
| Primary voltage ($V_{dc1}$) | 380 V |
| Prototype power capability ($P$) | 1.8 kW |
| Dead time ($t_d$) | 0.24 μs (3.5°) |
| Voltage ratio ($r = nV_{out}/V_{in}$) | 0.5 |
| Winding ratio ($N_P$:$N_S$) | 1:2 |
| Switching frequency ($f$) | 80 kHz |
| Total leakage inductance ($L$) | 62 μH |

### 2.5.2. Methodology

The experimental objectives of this chapter are to verify the ZVS operation of TDPWM and to compare the efficiency of CPWM and PSM. Both of the modulation strategies are implemented with a digital processor (TMS320F28335, TI). The power is controlled by manually shifting the fundamental phase shift from –90° to 90°. The efficiency, input, and output power of the prototype are measured with a precision power analyzer (WT1800, YOKOGAWA). The soft-switching operation in verified with an oscilloscope.

### 2.5.3. Results and discussion

Fig. 2.15 plots theoretical and experimented output power of CPWM varied with fundamental phase from –90° to 90°. The dashed line is the experimental value. The black line is the experimental value. Since the voltage ratio of this experiment is 0.5, the boundary of Interval 1 and Interval 2 is 45° and –45°. The theoretical value is calculated from (2.17) in Interval 1 and from (2.43) in Interval 2.

The characteristic of the power was nonlinear, and it has an S-shape graph for positive and negative power transfer. The gradient of the power was the highest at 45° and –45°. The gradient of the power was the lowest at –90°, 0°, and 90°. It is a challenge due to design the controller for CPWM due to the nonlinear power characteristic.

The theoretical positive and negative maximum powers were 1.6 kW and –1.5 kW, respectively. The overall experimental value was lower than the overall theoretical value ($P_{max}$=±1.8 kW). The lower experimental value was expected because all losses are neglected in the theoretical value.

The power transferred from FB1 to FB2 if the fundamental phase was positive ($\varphi_f$>0). The power transferred from FB2 to FB1 if the fundamental phase was negative ($\varphi_f$<0). This shows that the power has been transferred in the negative direction. This means that the power has been successfully transferred from the secondary side to the primary side with the proposed algorithm in Fig. 2.12. The experimental result confirms that CPWM has a wide operating range and bidirectional capability.

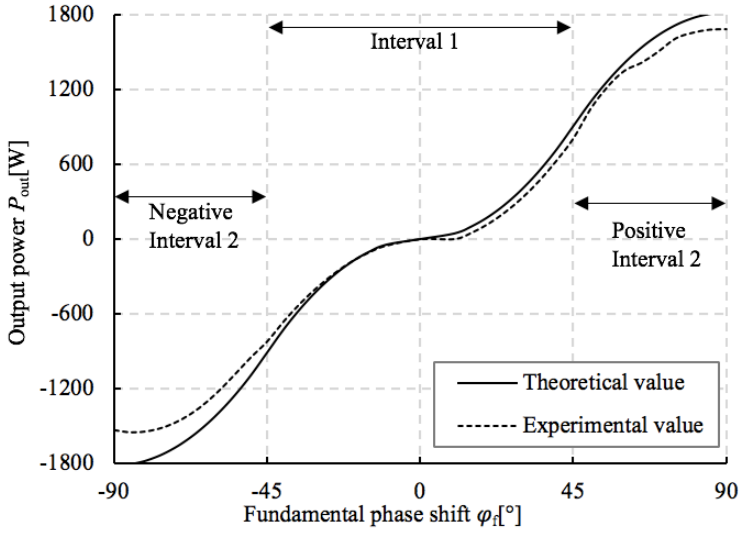



Fig. 2.15. Theoretical and experimental output power of CPWM varied with fundamental phase.

Fig. 2.16 shows experimental CPWM waveforms of the primary voltage width $v_P$, the product of the winding ratio and the secondary voltage width $nv_S$, and the primary inductance current $i_L$. The hard-switching points are marked with red circles. The waveforms are taken at four points in each interval ($P_{out}$= –1.4 kW, –0.6 kW, 0.6 kW, and 1.4 kW) to verify the reduction of circulating current.

Fig. 2.16(a) presents the waveform at the rated-power, $P_{out}$=600 W, and the selected fundamental phase, $\varphi_f$ = 40°, where the power is flowing from FB1 to FB2. As can be seen, the leakage inductance current at $i_L(0)$ and $i_L(\pi)$ satisfied the ZCS condition ($i_L(0)$ = 0, $i_L(\pi)$ = 0). The reduction of circulating current is confirmed with CPWM in the positive power transfer.

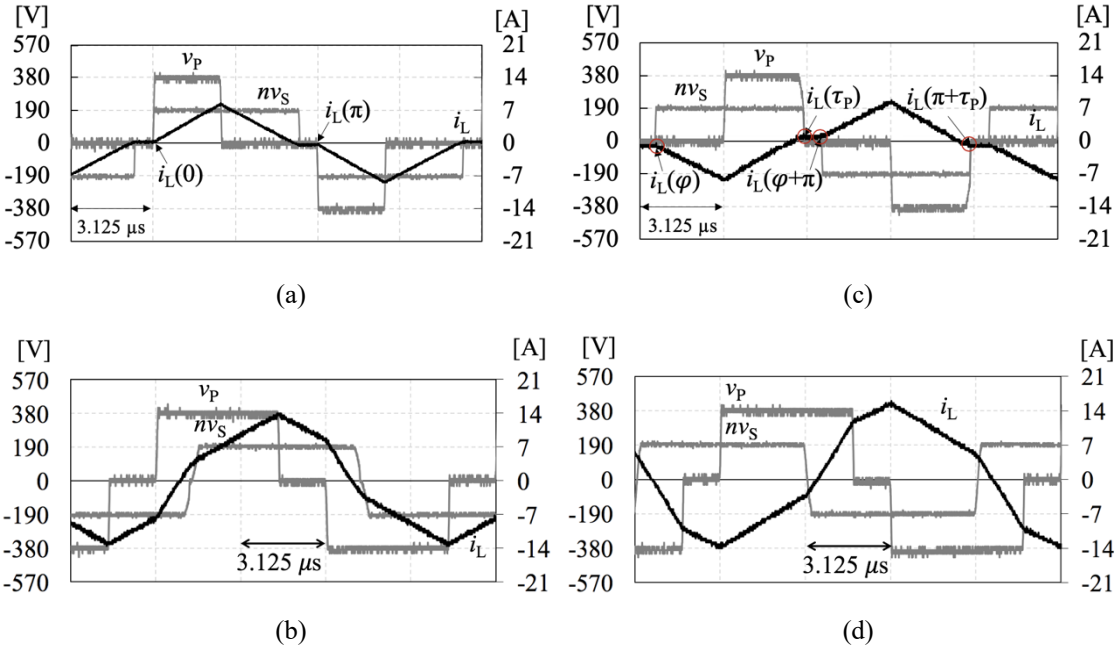



Fig. 2.16. Experimental waveforms of CPWM when (a) $\varphi_f$ = 40°, $P_{out}$ = 600 W. (b) $\varphi_f$ = 65°, $P_{out}$ = 1400 W. (c) $\varphi_f$ = –40°, $P_{out}$ = –600 W. (d) $\varphi_f$ = –70°, $P_{out}$ = 1400 W.

Fig. 2.16(c) is waveform at $P_{out}$=–600 W, $\varphi_f$ = –45°. The leakage current at $i_{L1}(\varphi)$, $i_{L1}(\tau_P)$, $i_{L1}(\varphi+\pi)$, and $i_{L1}(\tau_P+\pi)$ were not satisfying the ZCS condition ($i_{L1}(\varphi)$=0, $i_{L1}(\tau_P)$=0) and the ZVS condition ($i_{L1}(\varphi)$>0, $i_{L1}(\tau_P)$<0). The leakage current at $i_{L1}(\varphi)$ and $i_{L1}(\tau_P)$ were –1.2 A and 1.2 A, respectively. This means the power devices in legs 3 and 4 ($S_5$-$S_8$) were operating in hard-switching. Fig. 2.17 shows the experimental waveform at $i_{L1}(\tau_P)$. The hard-switching in leg 3 is confirmed by observing Fig. 2.17. The voltage of the primary voltage slight dropped earlier before $i_{L1}(\tau_P)$ and the leakage inductance current slightly increase from 0.4 A to 1.2 A. This could be explained by including the dead time and parasitic capacitance [50]. The primary voltage $v_P$ dropped 0.24 µs before $\tau_P$, which is the period of dead time, due to the energy of the inductance that discharge the parasitic capacitance in $S_3$. The slight voltage drops in the primary voltage $v_P$ had caused the leakage inductance current to increase from 0.4 A to 1.2 A during the dead time period

which prevents the power devices in legs 3 and 4 to operate in ZCS. The parasitic capacitance and dead time have to be considered in the analysis to prevent the hard-switching operation.

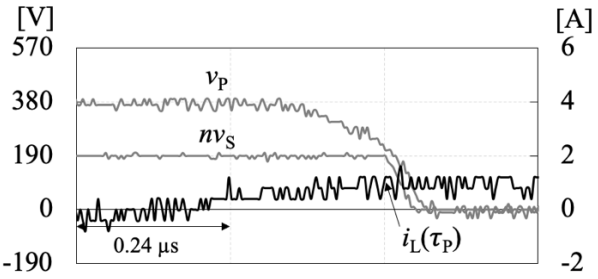



Fig. 2.17. Experimental waveforms at $i_L(\tau_P)$ when $\varphi_f = -40°$, $P_{out} = -600$ W.

Fig. 2.16(b) and (d) are waveforms at $P_{out}$=1400 W, $\varphi_f = 65°$ and $P_{out}$=–1400 W, $\varphi_f = -70°$, respectively. Both waveforms verify that CPWM is able to transfer bidirectional power in medium to high power range. All power devices were operating in soft-switching. There was no surge voltage found in the waveforms too.

Fig. 2.18 shows overall efficiency of PSM and CPWM varied with output power. The maximum efficiency of this converter is 93.7% at $P_{out}$=1.2 kW with CPWM. The overall efficiency of PSM when $r$=0.5 is below 90% at negative but has reached 90% at a part of positive power transfer (1.3 kW to 1.7 kW). The overall efficiency of CPWM has reached 90% at a part of negative (–1.5 kW to –0.4 kW) and a part of positive (0.7 kW to 1.6 kW) power transfer. The efficiencies of CPWM at –1.4 kW, –0.6 kW, 0.6 kW, and 1.4 kW are roughly 2%, 10%, 6%, and 3% above that of PSM, respectively. These results confirm that the reduction of the circulating current increases the efficiency of DAB converter in a voltage variation condition.

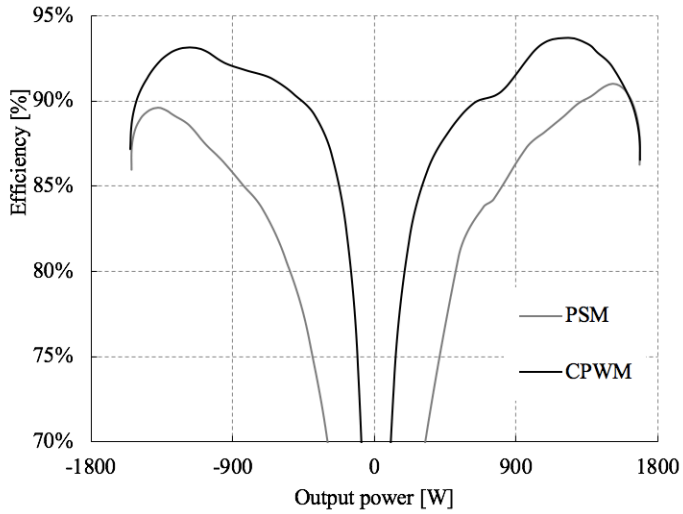



Fig. 2.18. Efficiency of PSM and CPWM varied with output power.

## 2.6. Conclusion

In this chapter, a simple modulation strategy with bidirectional, buck, and boost capability for the BESS is designed. In Section 2.1, twelve modulation strategies are selected and discussed to operate in a wide operational range and a wide voltage variation. Most of the modulation strategies are not suitable for the BESS. The suitable modulation strategy must have four qualities: simple, considers all degrees of freedom, bidirectional capability, and buck-boost operation capability.

To overcome these problems, DPWM and SPWM were analyzed in Section 2.3 with lossless DAB dc–dc model in Section 2.2. The analysis included inductance current, power transfer, and soft-switching conditions. The mathematical analysis of the soft-switching and power transfer of SPWM proves that SPWM is suitable for medium to high power transfer. The mathematical analysis of the soft-switching and power transfer of DPWM demonstrates that DPWM is suitable for low to medium power transfer.

Based on the analysis, a new modulation strategy, combined pulse-width modulation (CPWM), was proposed by combining DPWM and SPWM to enable the bidirectional power flow and the boost operations in Section 2.4. The CPWM algorithm combined the three degrees of freedom ($\varphi$, $\tau_P$, $\tau_S$) into the fundamental phase $\varphi_f$ and the voltage ratio $r$. The interval classification was defined and the algorithm for Interval 1, Interval 2, and buck operation were calculated.

The proposed modulation strategy, CPWM, was experimented with the first prototype in Section 2.5. The experimental results verified that CPWM has a wide operating range and bidirectional capability. The ZCS was verified in the positive Interval 1. However, hard-switching operations were found at legs 3 and 4 in the negative Interval 1 due to the parasitic elements. The soft-switching in all power devices were verified in positive and negative Interval 2. In addition, the efficiency of CPWM and PSM were compared. From the experimental results, the efficiency of CPWM at the low power transfer (±0.6 kW) is more than 6% higher than that of PSM. The superiority of CPWM to PSM was verified.

CPWM is suitable for DAB dc–dc converter even if the BESS is operating in a large voltage variation and a wide operational range. However, the reliability of the BESS with the algorithm in Fig. 2.12 is not verified. In reality, the lithium batteries always have voltage variation during the charge or discharge mode. A continuous operation test with the voltage variation conditions is essential to verify the reliability of the system. In the future, this test is needed to ensure the reliability of the algorithm before the BESS is tested with the real lithium batteries. In addition, the dead time and parasitic capacitance effects are not included in the analysis. The modulation strategy have to be analyzed with these parasitic elements to operate in the soft-switching.

# 3. Simple Modulation Strategy with ZVS Capability

## 3.1. Introduction

In the wide voltage variation condition, the DAB dc–dc converter has a limited ZVS range. Especially, the power devices operate in hard-switching at the low power range. Since the DAB dc–dc converter uses eight power devices, the hard-switching operation in the power devices increases the switching losses. Besides, the power devices have parasitic elements. In the hard-switching operation, these parasitic elements cause an additional snubber losses [51]. These losses can be reduced with ZVS operation [52]. The ZVS conditions are essential to design a high efficiency modulation strategy for the BESS.

There are many literatures focused on the modulation strategy to operate in soft-switching. CPWM has a wide operational range. However, CPWM has hard-switching operation in the low power range due to the parasitic capacitances and dead time effect [53], [49]. A previous research attempted to operate in ZVS with DPWM (low power range of CPWM) by considering the parasitic capacitances [54]. However, the literature did not include the dead time effect.

In this chapter, the modulation strategy with the parasitic capacitances and the dead time effects are analyzed to operate in ZVS.

## 3.2. DAB converter with parasitic components

The high switching frequency operation reduces the size of passive components in the DAB converter. Although the high switching frequency operation is possible with the latest power devices such as MOSFET, the parasitic capacitances of the MOSFET cause additional losses such as snubber loss and switching loss. These losses can be reduced with ZVS operation. In this section, the DAB converter with parasitic components are analyzed to operate in ZVS.

### 3.2.1. DAB converter configuration

Fig. 3.1 shows the configuration of dual active bridge (DAB) dc–dc converter with parasitic capacitances. In addition to the previous configuration, each power switch ($S_1$–$S_8$) has a parasitic capacitance.

The DAB converter has a natural capability to operate in ZVS. The parasitic capacitances reduce the ZVS operational range of the DAB converter. A power device operates in ZVS if it is turned on when the voltage between drain and source is zero. In order to achieve the ZVS, the parasitic capacitance in each

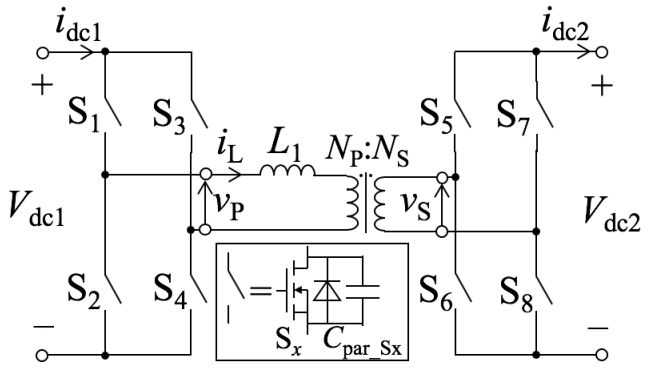



Fig. 3.1. Dual active bridge dc-dc converter with parasitic capacitance.

power device must be discharged before the power device is turned on. The failure to discharge the parasitic capacitance causes switching losses and snubber losses [51].

At the same time, the charge and discharge process slow the switching transition. Since the drain-source parasitic capacitance slightly takes time to charge or discharge, there is a finite time for the primary and secondary square voltages to change their voltage level (from 0 to $V_{dcx}$ or vice versa). The three levels of primary $v_p$ and secondary voltages $v_s$ with topology states are modified and summarized in Tables 3.1 and 3.2.

Table 3.1. Primary square voltage levels with dead time.

| | | |
|---|---|---|
| Primary square voltage $v_P(t)$ | $+V_{dc1}$ | State I : $S_1$, $S_4$ on, $S_2$, $S_3$ off |
| | $>>V_{dc1}$ | Trans. I+ : $S_4$ on, $S_1$, $S_2$, $S_3$ off |
| | $<<V_{dc1}$ | Trans. I– : $S_1$ on, $S_2$, $S_3$, $S_4$ off |
| | 0 | State II : $S_1$, $S_3$ on, $S_2$, $S_4$ off or<br>State III : $S_2$, $S_4$ on, $S_1$, $S_3$ off |
| | $<<-V_{dc1}$ | Trans. IV– : $S_2$ on, $S_1$, $S_3$, $S_4$ off |
| | $>>-V_{dc1}$ | Trans. IV+ : $S_3$ on, $S_1$, $S_2$, $S_4$ off |
| | $-V_{dc1}$ | State IV : $S_2$, $S_3$ on, $S_1$, $S_4$ off |

Table 3.2. Secondary square voltage levels with dead time.

| | | |
|---|---|---|
| Secondary square voltage $v_S(t)$ | $+V_{dc2}$ | State I : $S_5$, $S_8$ on, $S_6$, $S_7$ off |
| | $>>+V_{dc2}$ | Trans. I+ : $S_8$ on, $S_5$, $S_6$, $S_7$ off |
| | $<<+V_{dc2}$ | Trans. I– : $S_5$ on, $S_6$, $S_7$, $S_8$ off |
| | 0 | State II : $S_5$, $S_7$ on, $S_6$, $S_8$ off or<br>State III : $S_6$, $S_8$ on, $S_5$, $S_7$ off |
| | $<<-V_{dc2}$ | Trans. IV– : $S_6$ on, $S_5$, $S_7$, $S_8$ off |
| | $>>-V_{dc2}$ | Trans. IV+ : $S_7$ on, $S_5$, $S_6$, $S_8$ off |
| | $-V_{dc2}$ | State IV : $S_6$, $S_7$ on, $S_5$, $S_8$ off |

### 3.2.2. Modulation Strategy with dead-time

In addition to the switching transition, the nature of a power device is considered. In reality, every power device has a finite switching time. There is a delay in switching on and off the power devices. Especially, the turn-off delay may cause a short circuit during the switching transition of the power devices in the same leg. Therefore, it is essential to insert a dead time or to delay the turn-on signal to avoid the short circuit. Fig. 3.2 shows waveforms of a modulation strategy with dead time. Although the time delay guarantees safe operation, it effects the performance of the DAB converter [50]. The delay on the originally intended turn-on signal may affect the quality of the modulation strategy. The dead time effect is more significant in a high switching operation. In addition, Fig. 3.2 shows that the parasitic capacitances in the drain-source of the power devices slow down the switching transition. Although the parasitic capacitances and the dead time are present, the current value of the three degrees of freedom can be confirmed by observing the primary and secondary square voltages.

The dead time and parasitic capacitance are considered in the modulation strategy analysis to accurately operate in the DAB converter in the ZVS condition. Since in Section 3.3, the DAB converter has hard-switching only in Interval 1 of CPWM, only the ZVS condition of DPWM is analyzed.

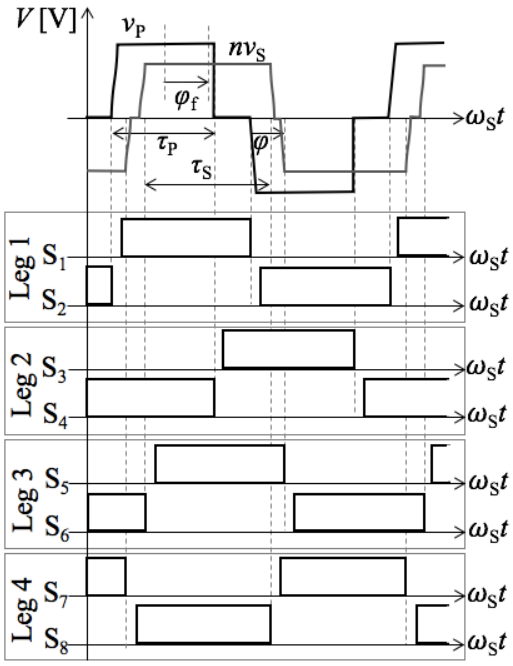



Fig. 3.2. Waveforms of a modulation strategy with dead time.

### 3.2.3. ZVS conditions of DPWM

Fig. 3.3 shows an example of a DPWM waveform where all the power devices are operating in ZVS. The dead time and switching transition are also considered in this waveform. In a ZVS operation, the switching transition occurs within the dead time period. The concept of operating DPWM in ZVS is

different from operating in ZCS. As can be seen, circulating current is needed to discharge the parasitic capacitance. The leakage inductance current conditions are the key to the ZVS operation for all power devices [52].

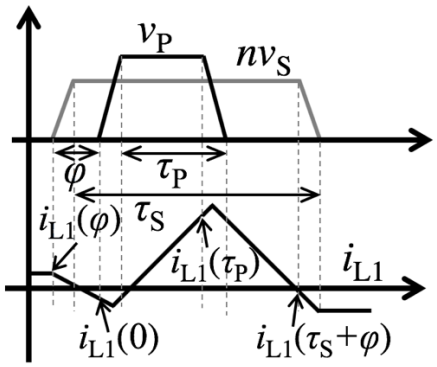



Fig. 3.3. The DPWM waveform with dead time.

From Section 2, the power devices have hard-switching in legs 1, 3, and 4 with DPWM. The leakage inductance current conditions in legs 1 and 3 are analyzed to operate in ZVS. Fig. 3.4 shows the ZVS operation during the dead time ($t_1$ to $t_2$) of legs 1 and 3. The ZVS is achieved when;

1. The parallel parasitic capacitance of $S_1$ and $S_5$ is completely discharged and
2. the current ($i_P$ or $i_S$) from the leakage inductance ($L_1$ or $L_1/n^2$) flows through the antiparallel diode of the power device ($S_1$ or $S_5$) before the power device ($S_1$ or $S_5$) is switched on at $t_2$.

The leakage inductance current gives the leakage inductance an energy to discharge the parasitic capacitance. For the ZVS operation, the energy in the leakage inductance has to be more than or equal to the energy in the parasitic capacitances (Noted that there are two parasitic capacitances to be discharged with one leakage inductance). The energy balance with the charge-equivalent capacitance [52] for legs 1 and 3 are

$$\frac{1}{2}L_1{i_P}^2(0) \geq C_{\text{par\_S1}}{V_{\text{dc1}}}^2, \tag{3.1}$$

and

$$\frac{1}{2n^2}L_1{i_S}^2(\varphi) \geq C_{\text{par\_S5}}{V_{\text{dc2}}}^2, \tag{3.2}$$

respectively, where $C_{\text{par\_S1}}$ is the parasitic capacitance of $S_1$, and $C_{\text{par\_S5}}$ is the parasitic capacitance of $S_5$. Each value of $C_{\text{par\_S1}}$ and $C_{\text{par\_S5}}$ includes the parasitic capacitance of the printed circuit board. The parasitic capacitance of the power devices in each bridge are assumed to be equal ($C_{\text{par\_S1}}=C_{\text{par\_S2}}=C_{\text{par\_S3}}=C_{\text{par\_S4}}$, $C_{\text{par\_S5}}=C_{\text{par\_S6}}=C_{\text{par\_S7}}=C_{\text{par\_S8}}$). The relationship between the primary current $i_{\text{P}}$ and the secondary current $i_{\text{S}}$ is

$$ni_{\text{P}} = i_{\text{S}}. \tag{3.3}$$

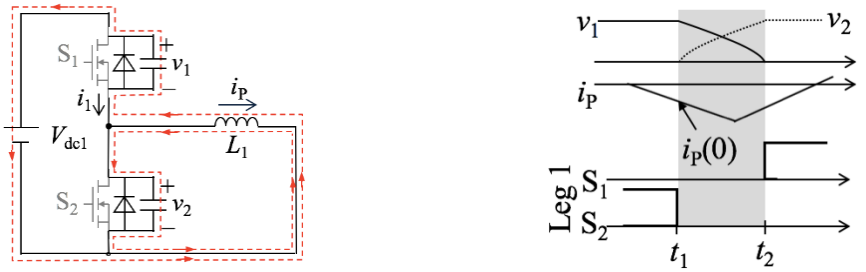
Since the parasitic capacitance of all power devices are the same, the leakage inductance current conditions for legs 1 and 3 are also applicable for legs 2 and 4. From (3.1), (3.2), and (3.3), the inductance current conditions for all legs to achieve ZVS are

$$i_{\text{P}}(0) \le -\sqrt{\frac{2C_{\text{par\_S1}}{V_{\text{dc1}}}^2}{L_1}}, \tag{3.4}$$

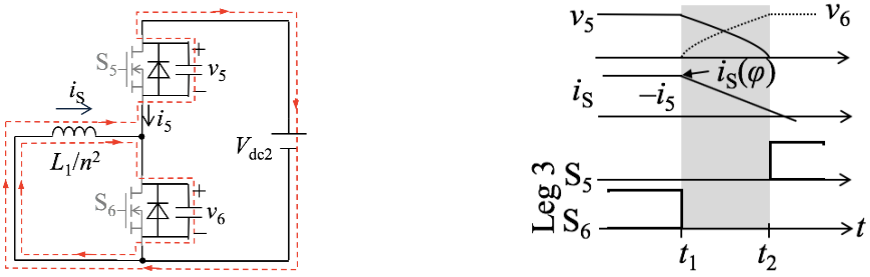
$$i_{\text{P}}(\varphi) \ge \sqrt{\frac{2C_{\text{par\_S5}}{V_{\text{dc2}}}^2}{L_1}}, \tag{3.5}$$

$$i_{\text{P}}\left(\tau_{\text{P}} + \varphi_{\text{dead}}\right) \ge \sqrt{\frac{2C_{\text{par\_S1}}{V_{\text{dc1}}}^2}{L_1}}, \tag{3.6}$$

and




(a) switching transition of leg 1 ($t_1$ to $t_2$).




(b) switching transition of leg 3 ($t_1$ to $t_2$).

Fig. 3.4. ZVS operation.

$$i_{\mathrm{P}}(\tau_{\mathrm{S}}+\varphi+\varphi_{\mathrm{dead}}) \le -\sqrt{\frac{2C_{\mathrm{par\_S5}}{V_{\mathrm{dc2}}}^{2}}{L_1}} \tag{3.7}$$

## 3.3. Tunable DPWM

As mentioned in the previous section, the ZVS operation depends on the leakage inductance current conditions. In this section, DPWM is analyzed and modified to satisfy the leakage inductance current conditions. Based on the analysis, tunable DPWM is proposed to operate in ZVS for buck and boost operation.

### 3.3.1. DPWM with dead time

In DPWM with dead time, from Tables 3.1 and 3.2, there are states I, II, III, IV, trans. I+,I–,IV+, and IV–, in primary square voltage and secondary square voltage. Fig. 3.5 shows a steady-state condition of dual pulse-width modulation waveforms where the voltages $v_{\mathrm{P}}(t)$ and $v_{\mathrm{S}}(t)$ and the leakage inductance current $i_{\mathrm{P}}(t)$ repeat every full cycle $T_{\mathrm{S}}$.

From (2.2), (2.7), time intervals I, II, III, IV, V, VI, and VII ($0 < t < T_{\mathrm{S}}/2$) in Fig. 3.5, the primary inductance current in the positive and negative power transfer can be expressed as:

$$\text{time interval I } \left(\frac{\varphi}{\omega_{\mathrm{S}}} \le t \le \frac{\varphi+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\varphi+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}\left(\frac{\varphi}{\omega_{\mathrm{S}}}\right) - \frac{nV_{\mathrm{dc2}}}{2\omega_{\mathrm{S}}L}\varphi_{\mathrm{dead}} \tag{3.8}$$

$$\text{time interval II } \left(\frac{\varphi+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}} \le t \le 0\right):\ i_{\mathrm{P}}(0) = i_{\mathrm{P}}\left(\frac{\varphi+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right) + \frac{nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}}L}(\varphi+\varphi_{\mathrm{dead}}) \tag{3.9}$$

$$\text{time interval III } \left(0 \le t \le \frac{\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}(0) + \frac{1}{\omega_{\mathrm{S}}L}\left(\frac{V_{\mathrm{dc1}}}{2} - nV_{\mathrm{dc2}}\right)\varphi_{\mathrm{dead}} \tag{3.10}$$

$$\text{time interval IV } \left(\frac{\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}} \le t \le \frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) = i_{\mathrm{P}}\left(\frac{\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right) + \frac{V_{\mathrm{dc1}} - nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}}L}(\tau_{\mathrm{P}} - \varphi_{\mathrm{dead}}) \tag{3.11}$$

$$\begin{aligned}\text{time interval V } &\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}} \le t \le \frac{\tau_{\mathrm{P}}+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right)\\ &= i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}}{\omega_{\mathrm{S}}}\right) + \frac{1}{\omega_{\mathrm{S}}L}\left(\frac{V_{\mathrm{dc1}}}{2} - nV_{\mathrm{dc2}}\right)\varphi_{\mathrm{dead}}\end{aligned} \tag{3.12}$$

$$\begin{aligned}\text{time interval VI } &\left(\frac{\tau_{\mathrm{P}}+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}} \le t \le \frac{\tau_{\mathrm{S}}+\varphi}{\omega_{\mathrm{S}}}\right):\ i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{S}}+\varphi}{\omega_{\mathrm{S}}}\right)\\ &= i_{\mathrm{P}}\left(\frac{\tau_{\mathrm{P}}+\varphi_{\mathrm{dead}}}{\omega_{\mathrm{S}}}\right) - \frac{nV_{\mathrm{dc2}}}{\omega_{\mathrm{S}}L}(\tau_{\mathrm{S}}+\varphi-\tau_{\mathrm{P}}-\varphi_{\mathrm{dead}})\end{aligned} \tag{3.13}$$

$$\text{time interval VII } \left(\frac{\tau_S+\varphi}{\omega_S} \le t \le \frac{\tau_S+\varphi+\varphi_{dead}}{\omega_S}\right):\ i_P\left(\frac{\tau_S+\varphi+\varphi_{dead}}{\omega_S}\right) = i_P\left(\frac{\tau_S+\varphi}{\omega_S}\right) - \frac{nV_{dc2}}{2\omega_S L}\varphi_{dead} \tag{3.14}$$

$$i_P\left(\frac{\varphi}{\omega_S}\right) = -i_P\left(\frac{\tau_S+\varphi+\varphi_{dead}}{\omega_S}\right). \tag{3.15}$$

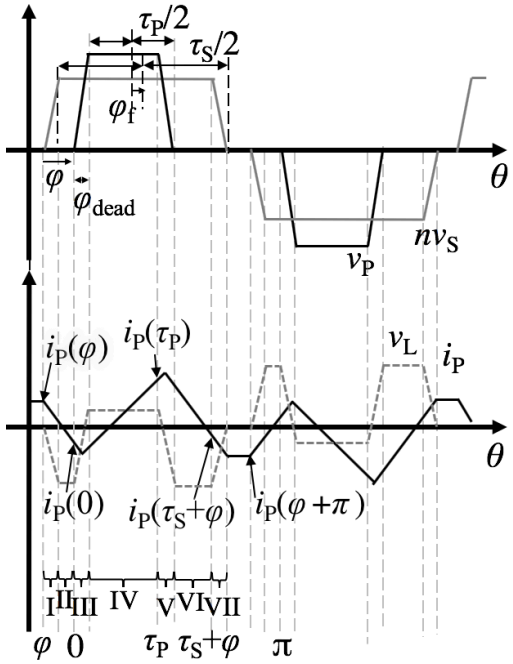



Fig. 3.5. Dual pulse-width modulation waveforms with dead time.

From (3.8), (3.9), (3.10), (3.11), (3.12), (3.13), (3.14), (3.15), and $\omega$=2$\pi$$f$s, the leakage inductance current at $\varphi$ is

$$i_P\left(\frac{\varphi}{\omega_S}\right) = \frac{nV_{dc2}\tau_S - V_{dc1}\tau_P}{2\omega_S L} \tag{3.16}$$

### 3.3.2. TDPWM algorithm

Based on the analysis in Item 3.2.2, the tunable DPWM (TDPWM) is proposed to operate the DAB converter in ZVS. In order to maintain the ZVS in the positive Interval 1, the three degrees of freedom are calculated based on the leakage inductance current conditions in (3.4) and (3.5). From (3.4), (3.5), (3.8), and (3.9), DPWM operates in the ZVS conditions at positive power transfer if the phase is

$$\varphi = -\frac{\omega L_1}{nV_{dc2}}\sqrt{\frac{2C_{par\_S1}{V_{dc1}}^2}{L_1}} - \frac{\omega L_1}{nV_{dc2}}\sqrt{\frac{2C_{par\_S5}{V_{dc2}}^2}{L_1}} - \frac{1}{2}\varphi_{dead}, \tag{3.17}$$

where the dead time is $\varphi_{\text{dead}} = (t_2 - t_1) \times 2\pi f_S$ [rad]. From (3.5) and (3.16), legs 3 and 4 operate in the ZVS if the primary voltage width is

$$\tau_P = r\tau_S - 2r\frac{\omega L_1}{nV_{dc2}}\sqrt{\frac{2C_{par\_S5}{V_{dc2}}^2}{L_1}}. \tag{3.18}$$

To simplify the ZVS conditions in (3.17) and (3.18), the parameters $\alpha_+$ and $\beta_+$ are used. The equations become

$$\varphi = -\alpha_+ - \beta_+, \tag{3.19}$$

and

$$\tau_P = r\tau_S - 2r\beta_+, \tag{3.20}$$

where the parameters $\alpha_+$ and $\beta_+$ are

$$\alpha_+ = \frac{\omega L_1}{nV_{dc2}}\left(\sqrt{\frac{2C_{par\_S1}{V_{dc1}}^2}{L_1}}\right) + \frac{1}{2}\varphi_{\text{dead}}, \tag{3.21}$$

and

$$\beta_+ = \frac{\omega L_1}{nV_{dc2}}\left(\sqrt{\frac{2C_{par\_S5}{V_{dc2}}^2}{L_1}}\right). \tag{3.22}$$

From (2.9), (3.19), and (3.20), the secondary voltage width is

$$\tau_S = \frac{2}{1-r}\left(\varphi_f + \alpha_+ + \beta_+(1-r)\right). \tag{3.23}$$

From (3.20) and (3.23), the primary voltage width is

$$\tau_P = \frac{2r}{1-r}(\varphi_f + \alpha_+). \tag{3.24}$$

For negative power transfer, the DAB converter operates in ZVS condition when the leakage conditions in (3.6) and (3.7) are satisfied. In addition, I assume that the parasitic capacitances charged rapidly at $i_{L1}(0)$. From (3.10) the time interval III becomes

$$\text{time interval III } \left(0 \le t \le \frac{\varphi_{\text{dead}}}{\omega_S}\right):\ i_P\left(\frac{\varphi_{\text{dead}}}{\omega_S}\right) = i_P(0) + \frac{V_{dc1} - nV_{dc2}}{\omega_S L}\varphi_{\text{dead}} \tag{3.25}$$

And the leakage inductance current at $\varphi$ becomes

$$i_P\left(\frac{\varphi}{\omega_S}\right) = \frac{nV_{dc2}\tau_S - V_{dc1}\tau_P - \frac{V_{dc1}\varphi_{\text{dead}}}{2}}{2\omega_S L} \tag{3.26}$$

From (2.9), (3.6), (3.7), (3.13), and (3.14), DPWM operates in the ZVS conditions at negative power transfer if the phase is

$$\varphi = 2\varphi_f - \frac{\omega L_1}{nV_{dc2}}\sqrt{\frac{2C_{par\_S1}{V_{dc1}}^2}{L_1}} - \frac{\omega L_1}{nV_{dc2}}\sqrt{\frac{2C_{par\_S5}{V_{dc2}}^2}{L_1}} - \frac{1}{2}\varphi_{\text{dead}}, \tag{3.27}$$

From (3.5) and (3.26), the ZVS conditions for legs 3 and 4 is

$$\tau_{\mathrm{P}} = r\tau_{\mathrm{S}} - 2r\left(\frac{\omega L_1}{nV_{\mathrm{dc2}}}\sqrt{\frac{2C_{\mathrm{par\_S5}}{V_{\mathrm{dc2}}}^2}{L_1}} + \frac{1}{4r}\varphi_{\mathrm{dead}}\right). \tag{3.28}$$

To simplify the ZVS conditions in (3.27) and (3.28), the parameters $\alpha_{-}$ and $\beta_{-}$ are used. The equations become

$$\varphi = 2\varphi_{\mathrm{f}} - \alpha_{-} - \beta_{-}, \tag{3.29}$$

and

$$\tau_{\mathrm{P}} = r\tau_{\mathrm{S}} - 2r\beta_{-}, \tag{3.30}$$

where the parameters $\alpha_{-}$ and $\beta_{-}$ are

$$\alpha_{-} = \frac{\omega L_1}{nV_{\mathrm{dc2}}}\left(\sqrt{\frac{2C_{\mathrm{par\_S1}}{V_{\mathrm{dc1}}}^2}{L_1}}\right) + \frac{1}{2}\varphi_{\mathrm{dead}} - \frac{1}{4r}\varphi_{\mathrm{dead}}, \tag{3.31}$$

and

$$\beta_{-} = \frac{\omega L_1}{nV_{\mathrm{dc2}}}\left(\sqrt{\frac{2C_{\mathrm{par\_S5}}{V_{\mathrm{dc2}}}^2}{L_1}}\right) + \frac{1}{4r}\varphi_{\mathrm{dead}}. \tag{3.32}$$

From (2.9), (3.29), and (3.30), the secondary voltage width is

$$\tau_{\mathrm{S}} = \frac{2}{1-r}\Big(-\varphi_{\mathrm{f}} + \alpha_{-} + \beta_{-}(1-r)\Big). \tag{3.33}$$

From (3.30) and (3.33), the primary voltage width is

$$\tau_{\mathrm{P}} = \frac{2r}{1-r}\big(-\varphi_{\mathrm{f}} + \alpha_{-}\big). \tag{3.34}$$

For the positive and negative Interval 1, the positive {(3.19), (3.23), (3.24)} and negative {(3.29), (3.33), (3.34)} equations of the three degrees of freedom are combined into

$$\varphi = \varphi_{\mathrm{f}} - |\varphi_{\mathrm{f}}| - \alpha - \beta, \tag{3.35}$$

$$\tau_{\mathrm{S}} = \frac{2}{1-r}\big(|\varphi_{\mathrm{f}}| + \alpha + \beta(1-r)\big), \tag{3.36}$$

$$\tau_{\mathrm{P}} = \frac{2r}{1-r}(|\varphi_{\mathrm{f}}| + \alpha), \tag{3.37}$$

where the parameters $\alpha$ and $\beta$ are

$$\alpha\begin{cases}\alpha_{+} & \text{if } \varphi_{\mathrm{f}} > 0\\ \alpha_{-} & \text{if } \varphi_{\mathrm{f}} < 0\end{cases}, \tag{3.38}$$

and

$$\beta\begin{cases}\beta_{+} & \text{if } \varphi_{\mathrm{f}} > 0\\ \beta_{-} & \text{if } \varphi_{\mathrm{f}} < 0\end{cases}, \tag{3.39}$$

respectively.

### 3.3.3. Boost (r>1) algorithm

In this case when the secondary voltage rises, which the voltage ratio becomes more than one, the algorithm of TDPWM is slightly different from that of $r$<1. As discussed in Item 2.4.4, the inverse voltage ratio is used instead of the original voltage ratio. In this condition, the primary voltage width must be larger than the secondary voltage width. The three degrees of freedom become

$$\varphi = \varphi_{\mathrm{f}} + |\varphi_{\mathrm{f}}| + \alpha + \beta, \tag{3.40}$$

$$\tau_{\mathrm{P}} = \frac{2}{1-r'}\left(|\varphi_{\mathrm{f}}| + \alpha + \beta(1-r')\right), \tag{3.41}$$

$$\tau_{\mathrm{S}} = \frac{2r'}{1-r'}(|\varphi_{\mathrm{f}}| + \alpha). \tag{3.42}$$

The equations of TDPWM for any values of the voltage ratio are summarized in Fig. 3.6. The proposed modulation strategy is experimented in next section.

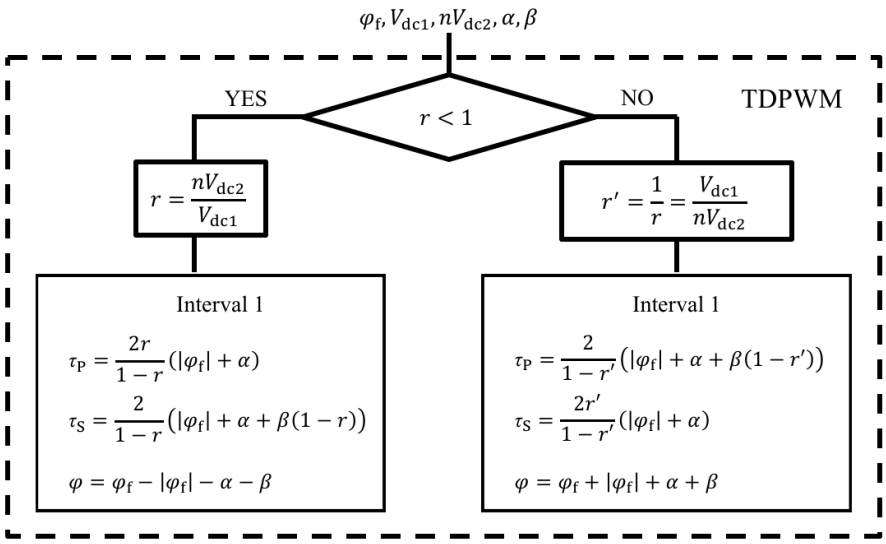



Fig. 3.6. Equations of the TDPWM strategy for any values of the voltage ratio.

## 3.4. Experiment

In this section, TDPWM are experimented using a new prototype to validate the ZVS operation in voltage variation conditions. Since the proposed modulation strategy only operates in low power transfer, a new prototype with appropriate parameters is designed for this chapter. The voltage ratios $r$=0.75 and $r$=1.27 are chosen to operate the converter in an unfavorable voltage variation scenario while the convenient condition is $r$=1.

### 3.4.1. Experimental parameters

The second prototype of the DAB converter is designed, and the configuration is shown in Fig. 3.8. The second prototype is shown in Fig. 3.7. The size is 33 cm × 37 cm × 6.5 cm. All the power devices are SiC MOSFETs. The core of the transformer is ferrite (PC40). The primary voltage is varied between 360 V and 400 V. The secondary voltage is varied between 150 V and 230 V. The primary to secondary winding ratio is 2:1. The total leakage inductance is 95 μH. In this case, the voltage ratio $r$ is varied between 0.75 and 1.27. The switching frequency is 50 kHz. The dead time is fixed at 0.33 μs. The parameters of the second prototype are summarized in Table 3.3.

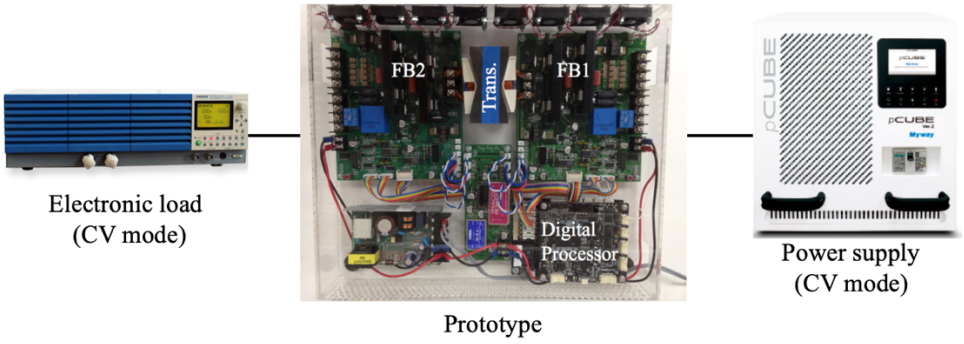



Fig. 3.7. The experimental set up of the DAB converter.

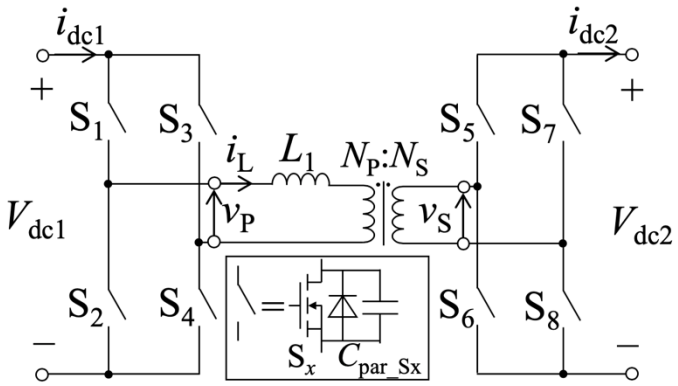



Fig. 3.8. The DAB converter configuration.

Table 3.3. Parameters of the second prototype.

| | |
|---|---|
| Primary voltage ($V_{dc1}$) | 360 V, 400 V |
| Secondary voltage ($V_{dc2}$) | 150 V, 230 V |
| Dead time ($t_d$) | 0.33 μs (5.94°) |
| Voltage ratio ($r = nV_{out}/V_{in}$) | 0.75, 1.27 |
| Winding ratio ($N_P$:$N_S$) | 2:1 |
| Switching frequency ($f$) | 50 kHz |
| Total leakage inductance ($L$) | 95 μH |

### 3.4.2. Methodology

The experimental objectives of this chapter are to verify the ZVS operation of TDPWM and to compare the efficiency of TDPWM and DPWM. Both of the modulation strategies are implemented with a digital processor (TMS320F28335, TI). The power is controlled by manually shifting the fundamental phase shift. The efficiency, input, and output power of the prototype are measured with a precision power analyzer (WT1800, YOKOGAWA). The ZVS operation in verified with an oscilloscope.

There are 4 sets of experiments that are summarized in Table 3.4.

Table 3.4. Sets of experiments.

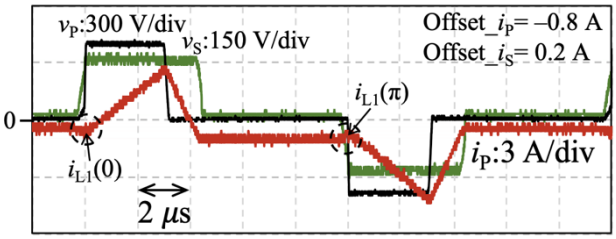
| | Parameters | Modulation strategy |
|---|---|---|
| Set 1 | $V_{dc1}$ = 400 V, $V_{dc2}$ = 150 V ($r$ = 0.75) | DPWM |
| Set 2 | $V_{dc1}$ = 360 V, $V_{dc2}$ = 230 V ($r$ = 1.27) | DPWM |
| Set 3 | $V_{dc1}$ = 400 V, $V_{dc2}$ = 150 V ($r$ = 0.75) | TDPWM |
| Set 4 | $V_{dc1}$ = 360 V, $V_{dc2}$ = 230 V ($r$ = 1.27) | TDPWM |

To satisfy the research objective, the sets are experimented as below:

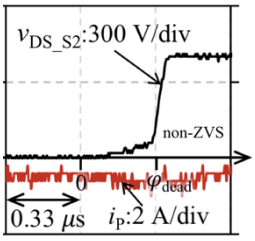
1. To verify the hard-switching of all power devices with DPWM at positive and negative power transfer in buck and boost condition with Set 1 and Set 2.
2. To verify the soft-switching of all power devices with TDPWM at positive and negative power transfer in buck and boost condition with Set 3 and Set 4.
3. To compare the efficiency of DPWM and TDPWM buck and boost condition with all sets.

### 3.4.3. Results and discussion

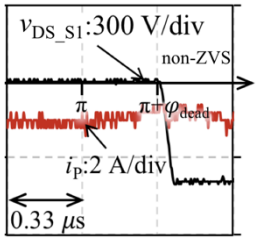
Fig. 3.9 shows the DPWM waveforms of Set 1 at a rated power 200 W, where the power is flowing from FB1 to FB2. The black line is the primary square voltage. The voltage range of the primary square voltage is 300 V/div. The green line is the secondary square voltage. The voltage range of the secondary square voltage is 150 V/div. The voltage scales of the primary and secondary sides are set differently in the experimental results to synchronize with the analysis in Section 3.2. To match with the analysis, the secondary square voltage scale is divided by the winding ratio. The red line is the primary current. The blue line is the secondary current. The circles indicate hard-switching points. Offset_$i_P$ and Offset_$i_S$ are the offset of the primary and the secondary current, respectively. Fig. 3.9(b) to (e) are the waveforms of the current and the voltage of a power device during dead time period. Fig. 3.9(a) shows that the DAB converter operated in hard-switching at $i_{L1}(0)$ and $i_{L1}(\pi)$. The hard-switching operation in leg 1 is confirmed by observing Fig. 3.9(b) and (c), where the leakage current at $i_{L1}(0)$ and $i_{L1}(\pi)$ were not satisfying the ZVS condition in Item 4.1.3. In Fig. 3.9(a), there was a –0.8 A offset on the primary current because the parasitic capacitances of the eight power devices have different values. Since the rate of charging and discharging of the charge depends on the parasitic capacitances, the leakage inductance current may have a positive or negative offset. This offset phenomenon has been also observed in a literature [55]. The offset phenomenon



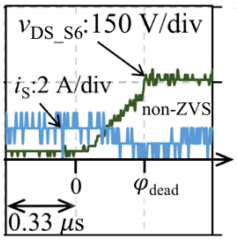

(a) One cycle waveform



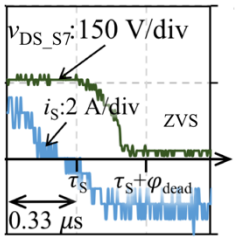

(b) Switching device $S_2$




(c) Switching device $S_1$




(d) Switching device $S_6$




(e) Switching device $S_7$

Fig. 3.9. The DPWM waveforms when

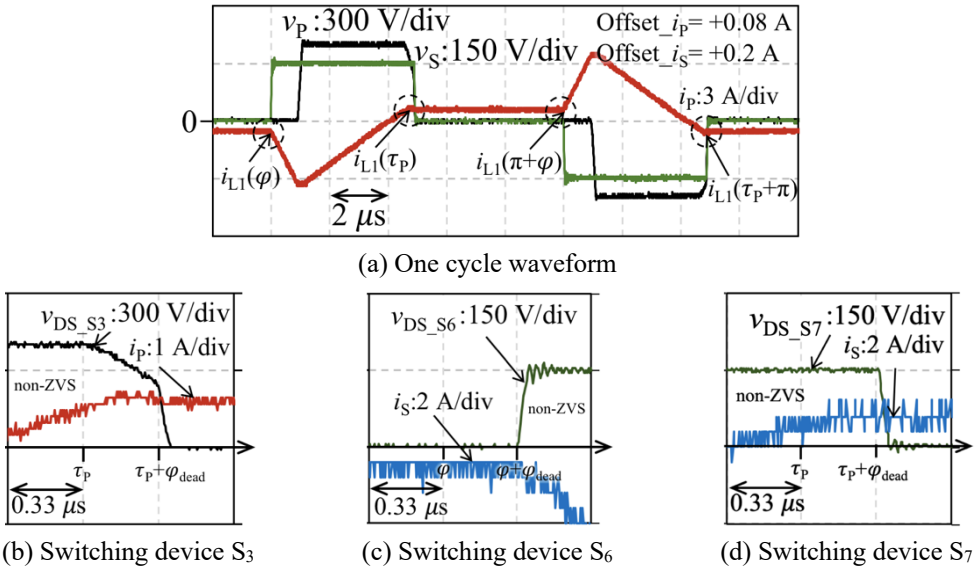
$V_{dc1}$ = 400 V, $V_{dc2}$ = 150 V ($r$ = 0.75), $P_O \approx$ 200 W, $\varphi_f$ = 10°, $\tau_P$ = 60°, $\tau_S$ = 80°.

has slightly increased the circulating current and discharged the parasitic capacitance in $S_1$ at $i_{L1}(0)$ but not enough to operate in ZVS. The offset of the secondary current was 0.2 A which was smaller than the primary current. The offset of the primary and secondary are very unpredictable in this experiment. Fig. 3.9(d) shows that the leakage inductance current was also insufficient to discharge the parasitic capacitance of leg 3 before the dead time ends. Fig. 3.9(e) shows that the parasitic capacitance at leg 4 was fully discharged during the dead time. Only the power devices in legs 2 and 4 were operating in ZVS during positive power transfer.

Fig. 3.10 shows the DPWM waveforms of Set 1 at a rated power –200 W, where the power is flowing from FB2 to FB1. Fig. 3.10(b) to (e) are the waveforms of the current and the voltage of a power device during dead time period. Fig. 3.10(a) shows that the DAB converter operated in hard-switching at $i_{L1}(\varphi)$, $i_{L1}(\tau_P)$, $i_{L1}(\varphi+\pi)$, and $i_{L1}(\tau_P+\pi)$.

The dead time effect is confirmed when the leakage inductance currents at $i_{L1}(\varphi)$ and $i_{L1}(\tau_P)$ were not zero. The hard-switching operation in leg 2 is confirmed by observing Fig. 3.10(b), where the leakage current at $i_{L1}(\varphi)$ was insufficient to discharge the parasitic capacitance before the dead time ends. The hard-switching operation in leg 3 and leg 4 are confirmed by observing Fig. 3.10(c) and (d), where the parasitic capacitances were not discharged during the dead time period.

Only the power devices in leg 1 was operating in ZVS during negative power transfer.




(a) One cycle waveform

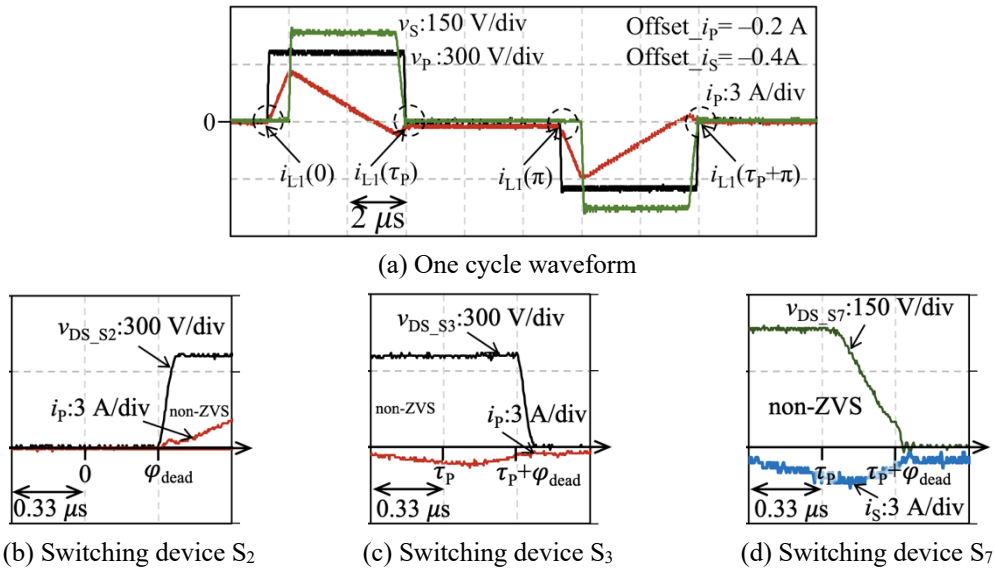
(b) Switching device $S_3$ (c) Switching device $S_6$ (d) Switching device $S_7$

Fig. 3.10. The DPWM waveforms when $V_{dc1}$ = 400 V, $V_{dc2}$ = 150 V ($r$ = 0.75), $P_O \approx$ –200 W, $\varphi_f$ = –11°, $\tau_P$ = 66°, $\tau_S$ = 88°.

Fig. 3.11 shows the DPWM waveforms of Set 2 at a rated power 200 W. Fig. 3.11(a) shows that the DAB converter operated in hard-switching at $i_{L1}(0)$, $i_{L1}(\tau_P)$, $i_{L1}(\pi)$, and $i_{L1}(\tau_P+\pi)$.

The hard-switching operation in leg 1 and 2 are confirmed by observing Fig. 3.11(b) and (c), where the parasitic capacitances were not discharged during the dead time period. The hard-switching operation in leg 4 is confirmed by observing Fig. 3.11(d), where the parasitic capacitance was not completely discharged during the dead time period.

Only the power devices in leg 1 was operating in ZVS during positive power transfer.




(a) One cycle waveform

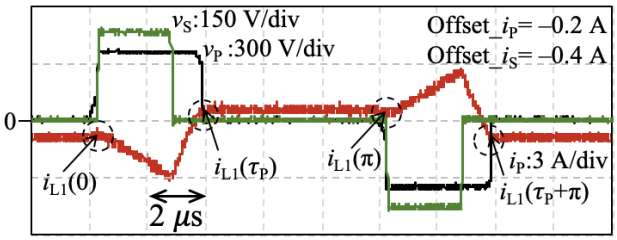
(b) Switching device $S_2$ (c) Switching device $S_3$ (d) Switching device $S_7$

Fig. 3.11. The DPWM waveforms when $V_{dc1}$ = 360 V, $V_{dc2}$ = 230 V ($r$ = 1.27), $P_O \approx$ 200 W, $\varphi_f$ = 9°, $\tau_P$ = 85°, $\tau_S$ = 67°.

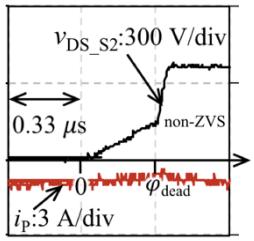
Fig. 3.12 shows the DPWM waveforms of Set 2 at a rated power –200 W. Fig. 3.12(a) shows that the DAB converter operated in hard-switching at $i_{L1}(0)$, $i_{L1}(\tau_P)$, $i_{L1}(\pi)$, and $i_{L1}(\tau_P+\pi)$. The dead time effect is confirmed when the leakage inductance currents at $i_{L1}(0)$ and $i_{L1}(\tau_P)$ were not zero.

The hard-switching operation in leg 1 and 2 are confirmed by observing Fig. 3.12(b) and (c), where the leakage inductance current was insufficient to discharge the parasitic capacitance before the dead time ends. The hard-switching operation in leg 3 is confirmed by observing Fig. 3.12(d), where the parasitic capacitance was not completely discharged during the dead time period.

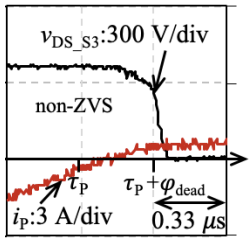
Only the power devices in leg 4 was operating in ZVS during positive power transfer.



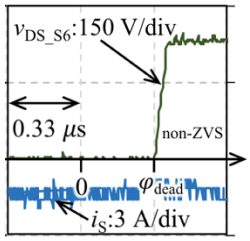

(a) One cycle waveform




(b) Switching device $S_2$




(c) Switching device $S_3$



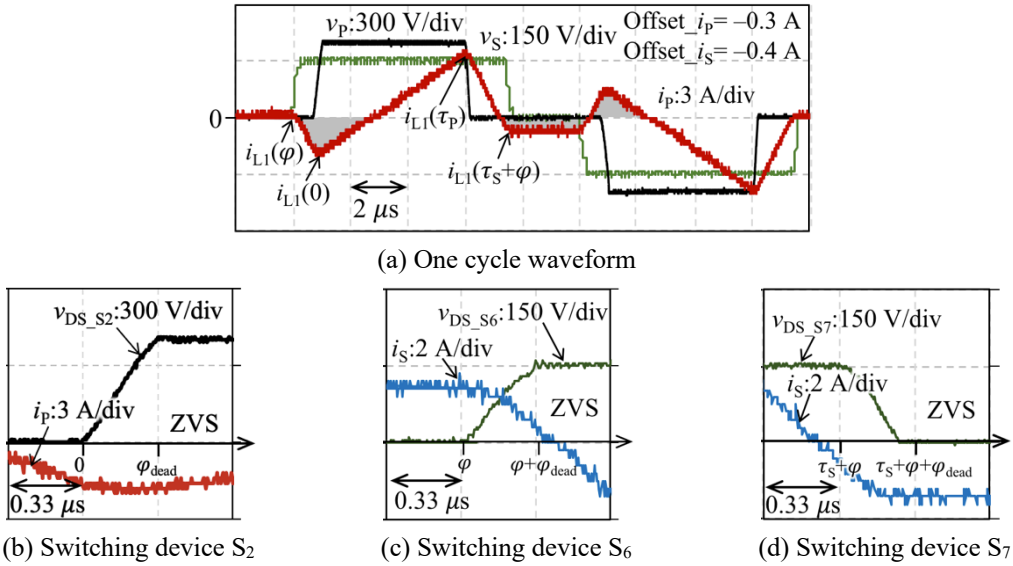

(d) Switching device $S_6$

Fig. 3.12. The DPWM waveforms when $V_{dc1}$ = 360 V, $V_{dc2}$ = 230 V ($r$ = 1.27), $P_O \approx$ –200 W, $\varphi_f$ = –7°, $\tau_P$ = 64°, $\tau_S$ = 50°.

Fig. 3.13 shows the TDPWM waveforms of Set 3 at a rated power 200 W. The grey shaded area is the circulating current. The leakage inductance current conditions have slightly increased the circulating current in the DAB converter.

Fig. 3.13(a) shows that the DAB converter operated in ZVS at all points. The soft-switching operation in leg 1 is confirmed by observing Fig. 3.13(b), where the parasitic capacitance was fully discharged before the dead time ends. The soft-switching operation in leg 3 is doubtful when it is observed from the primary current due to the –0.3 A offset in the primary current. However, Fig. 3.13(c) shows that the leakage inductance current at $i_S(\varphi)$ in the secondary current is enough to discharge the parasitic capacitance of $S_5$ before the dead time ends. From the secondary current perspective, the soft-switching operation in leg 3 and leg 4 are confirmed by observing Fig. 3.13(c) and (d), respectively.

All the power devices were operating in ZVS during positive power transfer with TDPWM if the parameters $\alpha$ and $\beta$ are 11 and 3, respectively.




(a) One cycle waveform

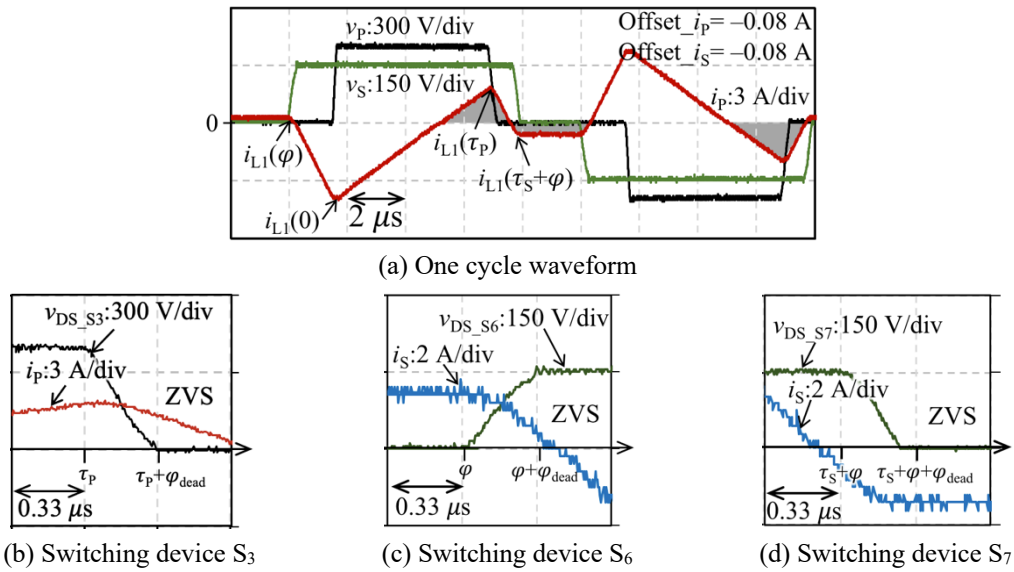
(b) Switching device $S_2$ (c) Switching device $S_6$ (d) Switching device $S_7$

Fig. 3.13. The TDPWM waveforms when $V_{dc1}$ = 400 V, and $V_{dc2}$ = 150 V ($r$ = 0.75), $P_O \approx$ 200 W, $\varphi_f$ = 5°, $\tau_P$ = 96°, $\tau_S$ = 134°, $\alpha$ = 11, $\beta$ = 3.

Fig. 3.14 shows the TDPWM waveforms of Set 3 at a rated power –200 W. Fig. 3.14(a) shows that the DAB converter operated in ZVS at all points.

The soft-switching operation in leg 2 is confirmed by observing Fig. 3.14(b), where the parasitic capacitance of $S_3$ was fully discharged before the dead time ends. The soft-switching operation in leg 3 is also doubtful when it is observed from the primary current due to the –0.08 A offset in the primary current. However, Fig. 3.14(c) verifies that the leakage inductance current at $i_S(\varphi)$ in the secondary current is enough to discharge the parasitic capacitance of $S_5$ before the dead time ends. From the secondary current perspective, the soft-switching operation in leg 3 and leg 4 are confirmed by observing Fig. 3.14(c) and (d), respectively.

All the power devices were operating in ZVS during negative power transfer with TDPWM if the parameters $\alpha$ and $\beta$ are 9 and 5, respectively.

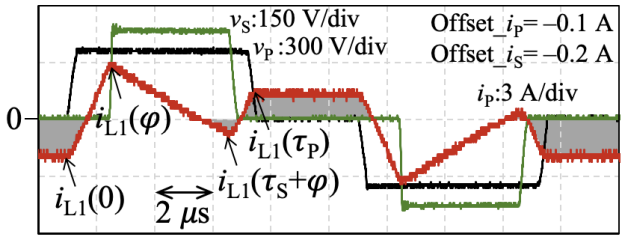



(a) One cycle waveform

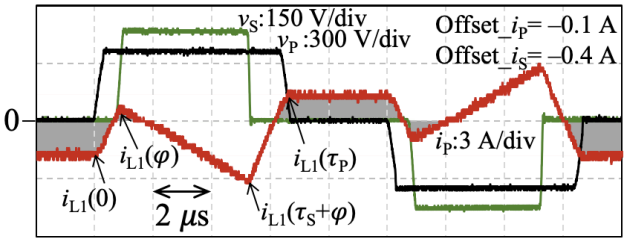
(b) Switching device $S_3$ (c) Switching device $S_6$ (d) Switching device $S_7$

Fig. 3.14. The TDPWM waveforms when $V_{dc1}$ = 400 V, and $V_{dc2}$ = 150 V ($r$ = 0.75), $P_O \approx$ –200 W, $\alpha$ = 9, $\beta$ = 5, $\varphi_f$ = –7°, $\tau_P$ = 96°, $\tau_P$ = 138°.

Fig. 3.15(a) and (b) show the TDPWM waveforms of Set 4 at the output power –200 W and 200 W, respectively. Fig. 3.15(a) shows the all the power devices operate in the ZVS during the positive power transfer with TDPWM if the parameters $\alpha$ and $\beta$ are 3 and 9, respectively. Fig. 3.15(b) shows the all the power devices operate in the ZVS during the negative power transfer with TDPWM if the parameters $\alpha$ and $\beta$ are 7 and 6, respectively. Both figures show that the ZVS is also possible for boost operation with TDPWM by tuning the parameters $\alpha$ and $\beta$.




(a) $P_O \approx 200$ W, $\alpha = 3$, $\beta = 9$, $\varphi_f = 7°$, $\tau_P = 112°$, $\tau_S = 74°$

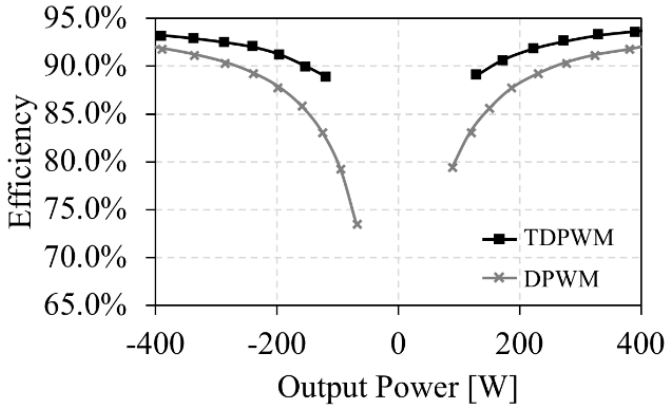



(b) $P_O \approx -200$ W, $\alpha = 7$, $\beta = 6$, $\varphi_f = -4°$, $\tau_P = 130°$, $\tau_S = 90°$

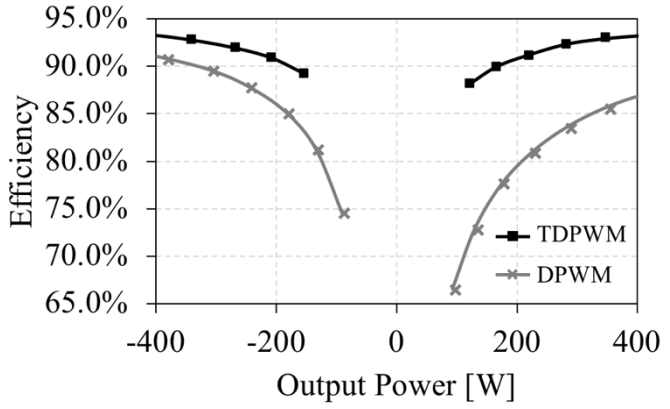
Fig. 3.15. The DPWM waveforms when $V_{dc1} = 360$ V, $V_{dc2} = 230$ V ($r = 1.27$).

Fig. 3.16(a) and (b) show the efficiency varied with the output power under voltage ratio 0.75 and 1.27, respectively. Fig. 3.16(a) shows that the overall efficiency of the DAB converter was higher with TDPWM than with DPWM under voltage ratio 0.75. The efficiency of TDPWM was 2% higher than that of DPWM at 400 W. Fig. 3.16(b) shows that the overall efficiency of the DAB converter was also higher with TDPWM than with DPWM under voltage ratio 1.27. The efficiency of TDPWM was 6% higher than that of DPWM at 400 W.

From the efficiency comparison of TDPWM and DPWM, the circulating current is needed to achieve ZVS resulting in higher efficiency regardless the voltage ratio. From the experimental results, the total loss from of the ZVS operation is lower than that of the switching losses and conduction losses.




(a) $V_{dc1}$ = 400 V, and $V_{dc2}$ = 150 V ($r$ = 0.75)




(b) $V_{dc1}$ = 360 V, $V_{dc2}$ = 230 V ($r$ = 1.27)

Fig. 3.16. Efficiency varied with the output power.

## 3.5. Conclusion

In this chapter, a simple modulation strategy with the ZVS capability in the low power range was designed. In Section 3.1, the low power range of CPWM (DPWM) has hard-switching operation due to dead time effect and parasitic components.

In Section 3.2, the DAB converter was analyzed with a parasitic capacitance in each power device. The parasitic capacitances caused additional snubber losses during the hard-switching operation and slowed down the switching transition even in the soft-switching operation. To operate in the ZVS operation, the parasitic capacitances have to be discharged before the power devices are turned on and off. The parasitic capacitances are fully discharged if the leakage inductance current is enough. The leakage inductance conditions were analyzed with the parasitic DAB converter.

To satisfy the leakage inductance current conditions, the DPWM algorithm was analyzed with the parasitic elements in Section 3.3. Based on the analysis, a new modulation strategy, tunable dual pulse-width modulation (TDPWM), was proposed to operate in the ZVS in the low power transfer for buck and boost conditions.

Lastly, TDPWM was experimented using the second prototype to validate the ZVS operation in Section 3.4. The experiments were done in large voltage variations. The experimental results verified TDPWM operated in the ZVS, and the efficiency of TDPWM at the low power transfer (±0.2 kW) was more than 3% higher than DPWM.

TDPWM is suitable for DAB dc–dc converter if the BESS is operating in a large voltage variation and a low power range.

# 4. Conclusion

In this study, the suitable modulation strategies of the dual active bridge (DAB) dc–dc converter are investigated for the battery energy storage system (BESS). The performance of the DAB converter depends on the modulation strategy.

In **Chapter 1**, the global trend of electrical energy showed that the BESSs are essential to increase the reliability of the renewable energies. Since bidirectional dc–dc converter is essential for the BESS, the dual active bridge (DAB) dc–dc converter was chosen due to the natural soft-switching capability, bidirectional buck-boost operation, and simple circuit configuration. There are two challenges to operate the DAB dc–dc converter in the BESS: large voltage variation and wide operational range.

In **Chapter 2**, the existent modulation strategies were investigated to operate in a large voltage variation and a wide operational range. Twelve modulation strategies were analyzed. However, they were not suitable for the BESS. The suitable modulation strategy must have four qualities: simple, consider all degrees of freedom, bidirectional capability and buck-boost operation capability. SPWM and DPWM were analyzed with a lossless DAB converter model. Based on the analysis, a new modulation strategy, combined pulse-width modulation (CPWM) was proposed with all the four qualities. CPWM was experimented using the first prototype in a large voltage variation. The experimental results verified that CPWM operate in a wide power transfer and bidirectional power transfer. Furthermore, the efficiency of CPWM and PSM was compared. The efficiency of CPWM at the low power transfer (±0.6 kW) was more than 6% higher than that of PSM. From these, the superiority of CPWM for the BESS to PSM was verified. Therefore, CPWM is suitable for DAB dc–dc converter if the BESS is operating in a large voltage variation and a wide operational range. However, there was hard-switching operation in the low power range (DPWM) due to the parasitic elements.

In **Chapter 3**, the effects of parasitic components and dead time were investigated in the DAB dc–dc converter model and in DPWM. The parasitic components caused additional snubber losses during the hard-switching operation, and the dead time slowed down the switching transition even in the soft-switching operation. The snubber losses are reduced if all power devices are operating in the ZVS. The ZVS operation depends on the leakage inductance conditions. To satisfy the leakage inductance conditions, DPWM is analyzed with the parasitic components and dead time effects. Based on the analysis, I e

have proposed tunable dual pulse-width modulation (TDPWM) to perform ZVS in the low power range for buck and boost conditions. TDPWM and DPWM were experimented using the second prototype in large voltage variation conditions. Several power devices were operating in hard-switching with DPWM.

The experimental results verified TDPWM operated in the ZVS, and the efficiency of TDPWM at the low power transfer (±0.2 kW) was more than 3% higher than DPWM.

CPWM is suitable for DAB dc–dc converter if the BESS is operating in a large voltage variation and a wide operational range. If the BESS only operates in the low power range and a large voltage variation, the DAB dc–dc converter has higher efficiency with TDPWM. The mixture of these modulation strategies is useful to achieve higher efficiency in the targeted operational range.

The originality of this study is the proposed algorithms increases the efficiency by reducing the circulating current and operating in the soft-switching in the positive and negative power transfer. There are no other modulation strategies that can transfer bidirectional power flow with a single algorithm. In reality, the algorithms of the modulation strategy are helpful in designing the programming of the digital processor for the DAB dc–dc converter.

In the future, the stability analysis of these modulation strategies is needed to design the controller of the DAB converter. A stable controller is essential when the BESS is connected to the power grid. In addition, the DAB converter designs, such as transformer designs and heat sink designs, should be optimized based on these modulation strategies to increase the converter's performance.

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# Research Achievement

## Transactions

1. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano, Kiyotsugu Takaba
   "Dual Active Bridge DC–DC Converter with Tunable Dual Pulse–Width Modulation for Complete Zero Voltage Switching Operation," IEEJ Journal of Industry Applications, vol. 8, no. 1, 2019
2. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano, Kiyotsugu Takaba
   "Combined Pulse–Width Modulation of Dual Active Bridge DC–DC Converter to Increase the Efficiency of Bidirectional Power Transfer," IEEJ Journal of Industry Applications, vol. 7, no. 2, pp. 166-174, March 2018

## International Conferences

1. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano, Kiyotsugu Takaba
   "Combined Pulse–Width Modulation of Dual Active Bridge DC–DC Converter to Reduce Circulating Current at Bidirectional Power Transfer," 2017 Joint Academic Forum at Danang, Vietnam, December 2017
2. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano, Kiyotsugu Takaba
   "Modulation Strategy of Dual Active Bridge DC–DC Converter for a Complete Zero Voltage Switching Operation," EPE'17 ECCE Europe – 19th European Conference on Power Electronics and Applications at Warsaw, Poland, September 2017
3. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano, Kiyotsugu Takaba
   "Control Strategy of Dual Active Bridge DC–DC Converter for Enhancing Zero Voltage Switching Operation," ICEE 2016 – The International Conference on Electrical Engineering at Okinawa, Japan, July 2016
4. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano
   "Fundamental Study on Control Strategies to Increase Efficiency of Dual Active Bridge DC-DC Converter," IECON 2015 – 41st Annual Conference of the IEEE at Yokohama, Japan, December 2015

## Domestic Conferences

1. Muhammad Hazarul Azmeer bin Ab Malek, Hiroaki Kakigano
   "Fundamental Study on Control Strategies to Increase Efficiency of Dual Active Bridge DC-DC Converter," 2015 Annual Meeting Record IEEJ, March 2015

# Award

1. Best presentation recognition at IECON 2015 in Yokohama, Japan by IECON 2015 Organization Committee.
    - Paper: “Fundamental Study on Control Strategies to Increase Efficiency of Dual Active Bridge DC-DC Converter”.