A Study on high performance and new functional dynamic type memory

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Dynamic Random Access Memory (DRAM) which realizes smaller macro size and larger memory capacity is extensively embedded on large scale and high performance System-on-Chip (SoC) in information-communication system. However, DRAM is facing the following issues: 1) Difficulty of operating voltage scale down on SoC platform of which power lowering is being driven by scaling down process technology, 2) Diminishing of the advantage of small macro size in small memory capacity range due to the area overhead of the power module, 3) Manufacturing cost increase due to the built-in special process steps into the standard CMOS process, 4) Difficulty of application to battery-powered mobile application which requires ultra-low power standby function with retaining the stored data, 5) Flexibility to realize the functions of operations and data comparison other than normal memory operation. To solve the issues of 1) and 2), Design For Manufacturability (DFM) - RAM introducing the 2Cell/bit - new memory architecture, where the bit data are expressed as the complimentary data stored in the coupled memory cells, is devised. To solve the issues of 2) and 3), on Silicon-On-Insulator (SOI) of which use for SoC started beyond 90nm era, capacitorless Twin-Transistor (TT) RAM, which stores the bit data in the change of floating body potential of SOI transistors, is devised. To solve the issue of 4), Power-Cut scheme introducing a unique deep standby state retaining the stored data, where the refresh operation and the internal power-off and power-resume are repeated, is devised. To solve the issue of 5), Multi-Function Programmable SOI - Memory (MFPM), which can be reconfigured to buffer memory, operational function memory, and content-addressable memory according to its use, is devised. As stated above, this study solves the issues of 1) to 5) on SoC-dynamic type memory adopting the new memory cell structure and additional novel circuits.