A study on reliability enhancement of power and circuit operation in VLSI

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With the advent of the deep submicron age, it becomes possible to implement high performance and large-scale system LSIs. At the same time, there are problems of signal integrity and power integrity, and manufacturing variation of transistor size and threshold voltage are increasing. These trends make dependable operation of LSI circuit difficult. To improve the dependability of the circuit operation of LSI, it is so necessary to construct a robust power design methodology that the circuit doesn't malfunction even when the manufacturing variation is caused.

First, a power design optimization method that can obtain an optimal solution with high dependability as a whole circuit is proposed even when the manufacturing variation is caused. The method not only treats IR drop, the electro migration and the wiring area, etc. as constraints but also aims to obtain a safer solution than a design constraint satisfaction. The common concept like design risk and safety is introduced for these plural design goals that exist in the trade-off relation, and high safety can be secured by the multi-objective optimization.

Next, a power design optimization that can consider the circuit delay variation due to the manufacturing variation and IR drop is implemented. The new design risk indicates ratio in danger which causes the manufacturing variation, IR drop and timing error, and a modeling method that relates among them is constructed. Therefore a power design optimization observing timing error risk directly can be implemented. In addition, another one observing timing error risk of critical path directly is implemented by combining with the statistical static timing analysis.

This effectiveness is shown by the experiments. As a result, since a power design optimization that considers the circuit delay variation due to the manufacturing variation and IR drop is implemented, the power design methodology can be achieved robustness and high reliability.