Abstract of Doctoral Thesis

Title：Study on Mask Programmable Devices for Low-Cost Fabrication and Intellectual Property Protection

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SoC (System on a Chip), which implement various hardware circuits into a single chip, have been successfully developed by the progress of miniaturization and integration technology of semiconductor device. In addition, LSI designer can manufacture semiconductor chip without owning a fabrication plant by outsourcing to the foundry, which is specialized on chip-making. On the other hand, the initial cost for mass-production, which includes LSI design and photo-mask, is increasing.
Recently, reverse-engineering is emerging as a serious problem. LSI design information, which is the valuable intellectual property, is exploited and illegally copied as a fake.

In this study, we focused on the mask programmable device (MPD) technology as a new approach to solve these problems. MPD is the design and fabrication technology which realize different operation, system and performance by changing only few photo masks among full mask-sets. Two types of MPD have proposed in this thesis.

Firstly, the device called Via Programmable Structured ASIC (VPSA), in which various digital circuits can be implemented by changing only via mask, is proposed. This device can reduce the initial costs of small-production volume LSI. The novel VPSA named “Via programmable device using EXclusive-or logic array (VPEX)” was presented in 2008 from our laboratory. In this study, we propose the new VPEX3 architecture which achieve area reduction and low power consumption than previous VPEX. The chip area of VPEX3 is reduced to about one third as shown in the evaluation of benchmark circuit. In order to show the usefulness of VPEX3, we construct dedicated CAD framework for VPEX3, and fabricate the prototype devices. The test chip is successfully operated. In order to solve the problem of lack of routing resources in VPEX3, VPEX4 is newly proposed. The area efficiency of VPEX4 is improved twice when large-scale circuit is implemented.

Secondly, Diffusion Programmable Device (DPD) is proposed. In this device, any

logic gate can be configured by changing the N-type / P-type in diffusion layer. Diffusion layer is located at the lowest layer in the LSI structure. Therefore the cost to analyze the diffusion structure is increased, because many upper layers have to be removed. In addition, the discrimination of the N-type / P-type using an optical microscope is considered to be very difficult. Therefore, DPD device will be useful to protect the Intellectual Property. The logic elements using the DPD was produced, and analyzed by optical microscope and scanning electron microscope. As a result, optical microscope cannot discriminate diffusion type. The scanning electron microscope can discriminate N-type/P-type at the specific observation condition, however, it requires large analysis cost. From these results, DPD is confirmed to have a resistance against reverse engineering.