主　論　文　要　旨

論文題名　**An Accurate Resister Transfer Level Power Macro-model in VLSI**

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主論文要旨

High performance and low power consumption are important requirements for modern embedded systems, and especially low power design is crucial for a battery driven mobile systems. In order to achieve accurate power estimation, the power estimation in highly abstraction level is necessary.

This thesis proposes an accurate resister transfer level (RTL) power macro-model to estimate the power consumption by analyzing the input data characteristics. In order to realize accurate power estimation, this thesis investigates the RTL power macro-model from two points: characterization and modeling.

In terms of characterization, first new parameter is proposed. To realize accurate power estimation, the parameter, which highly correlates with power consumption, is important. The proposed parameter characterizes the gate-level switching activities of the circuit, and aims to improve the estimation accuracy.

In terms of modeling, first conventional power macro-models including table-based method are improved. This thesis proposes two methods: table reference method considering power library unevenness and power estimation method using local area fitting.

Then, new power macro-model named power contour model is proposed. The power contour model is composed of a set of power contours, and each power contour takes the same power consumption. The power estimation is realized by interpolating corresponding two power contours. The experimental results show the proposed power contour model reduces max error 56.19% in maximum for 8 benchmark circuits, comparing to conventional method. RMS error is also improved 3.41% in maximum.